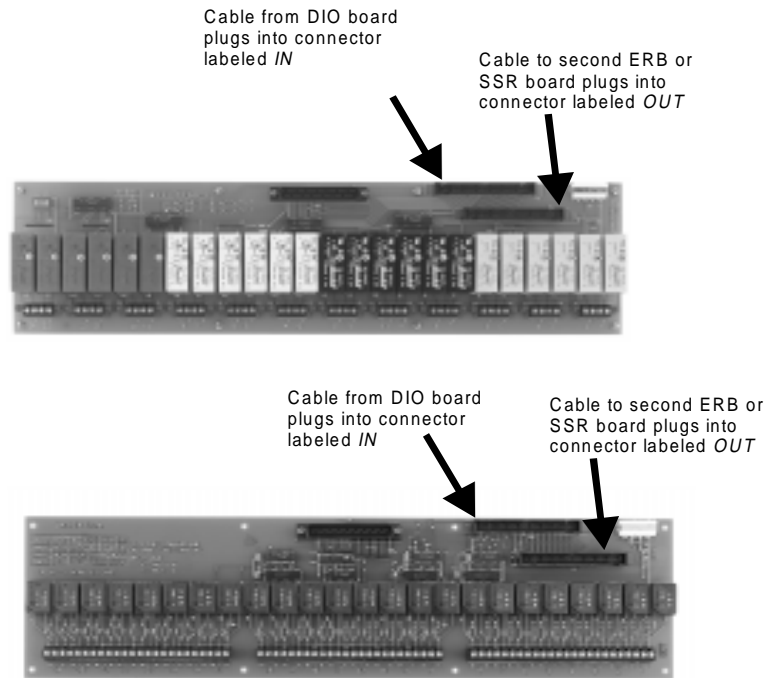


User's Guide

<http://www.omega.com>
e-mail: info@omega.com

CIO-DIO48
CIO-DIO48H
CIO-DIO96
CIO-DIO192



CIO-ERB-24 and SSR-RACK24 provide connectors allowing a single CIO-DIO-48 style board to control or monitor two 24-bit relay/SSR boards.

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INTRODUCTION

This manual provides complete information on CIO-DIO48, CIO-DIO48H, CIO-DIO96 and CIO-DIO192 digital I/O boards and accessories. The manual is organized into separate sections for those aspects of a product which are unique. Some issues, such as BASIC programming and electronic interfacing are applicable to all of the digital boards.

The CIO-DIO48 has two 82C55 parallel interface chips and a 50 pin connector. Each 82C55 controls 24 CMOS/TTLcompatible digital I/O pins. Within each 82C55, the digital I/O lines may be programmed as groups of 8,8 & 8 or 8,8 & 4,4. Each group may be input or output.

The CIO-DIO96 provides two CIO-DIO48 circuits on a single board while the CIO-DIO192 provides 4 CIO-DIO48 circuits on a single board. The CIO-DIO48H is a high drive, 48 line digital I/O board built up of logic chips. The control registers which set the direction of the I/O ports are identical to 82C55 mode 0 control registers (like those on the CIO-DIO48 in mode 0). The I/O lines are high drive, capable of sourcing 15mA and sinking 64mA.

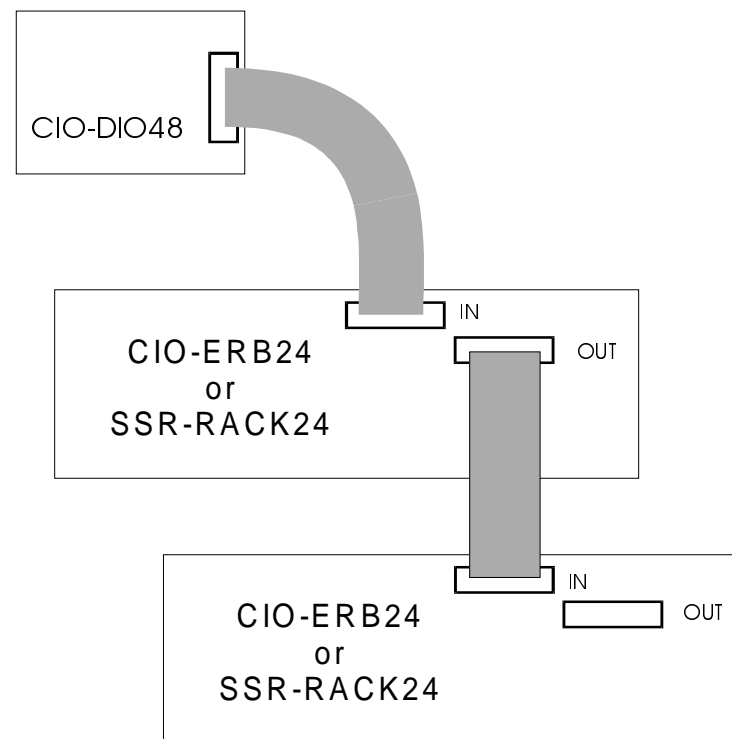
Each of the boards have the same connector pin-out and respond to the same software instructions. This manual includes information on programming the 82C55 in mode 0. Those wishing to use the 82C55 in modes 1 or 2 must procure a data book from Intel Corporation Literature Department.

The boards may either be programmed with direct I/O register reads and writes, or all mode 0 functionality is provided by the optional UniversalLibrary driver software.

The goal of this manual is to assist you in your application of a CIO board to your sensing or control problem. We are interested in your corrections and suggestions and will implement them.

CIO-ERB24 & SSR-RACK24 CONNECTIONS

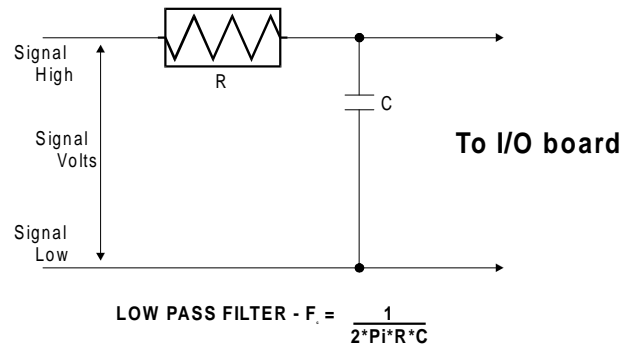
CIO-DIO48 family boards each provide digital I/O in groups of 48 bits. However, the most popular relay and SSR boards provide only 24-bits of I/O. The CIO-ERB24 and SSR-RACK24 each implement a connector scheme where all 48 bits of the CIO-DIO board may be used to monitor and control relays and/or SSRs. This configuration is shown in the block diagram below. The 24-bits of digital I/O on CIO-DIO connector pins 1-50 (base address +0 through +3) control the first relay board. The 24-bits of CIO-DIO on pins 51-100 will control the second relay/SSR board on the daisy chain.



A low pass filter is placed on the signal wires between a signal and an A/D board. It stops frequencies greater than the cut off frequency from entering the A/D board's analog or digital inputs.

The key term in a low pass filter circuit is cut off frequency. The cut off frequency is that frequency above which no variation of voltage with respect to time may enter the circuit. For example, if a low pass filter had a cut off frequency of 30 Hz, the kind of interference associated with line voltage (60Hz) would be filtered out but a signal of 25Hz would be allowed to pass.

Also, in a digital circuit, a low pass filter might be used to de-bounce an input from a momentary contact button pushed by a person.



A low pass filter may be constructed from one resistor (R) and one capacitor (C). The cut off frequency is determined according to the formula:

$$F_c = \frac{1}{2 * \text{Pi} * R * C}$$

$$R = \frac{1}{2 * \text{Pi} * C * F_c}$$

Where Pi = 3.14

The installation and operation of all three of the CIO-DIO series boards is very similar. Throughout this manual we use CIO-DIO as a generic designation for the CIO-DIO48, CIO-DIO48H, CIO-DIO96 and CIO-DIO192. When required due to the differences in the boards, the specific board name is used.

The CIO-DIO boards are easy to use. This quick start procedure will help you quickly and easily setup, install and test your board. We assume you already know how to open the PC and install expansion boards. If you are unfamiliar or uncomfortable with board installation, please refer to your computer's documentation.

*We recommend you perform the software installation described in sections 1.1 and 1.2 below prior to installing the board in your computer. The **InstaCal**TM operations below will show you how to properly set the switches and jumpers on the board prior to physically installing the board in your computer.*

INSTALL THE INSTACALTM SOFTWARE

Windows 95, 98 or NT users install the program by running the setup.exe program supplied with your DIO software. (DOS and Windows 3.x users need to run INTSTALL.EXE) It will create all required folders/directories and unpack the various pieces of compressed software. Simply run install and follow the on-screen instructions. Remember where the installed files are placed, as you will need to access them in the next step (the default location is on your main hard drive in a directory or folder named C:\CB\).

RUN INSTACALTM

To run **InstaCal**TM in the various forms of Windows, find the file named InstaCal.exe using your file management system and double click your mouse on it. In DOS simply type *instacal* and press the *Enter* key.

Once running, **InstaCal**TM provides four sub-menus (plus exit).

1. Select **Install** (either highlight it and hit enter or double click your mouse on it).

2. Select **Board #0** (select another number if Board #0 is already installed)
3. Select **Board Type**
4. Move through the selections and highlight the particular board you are installing (e.g. CIO-DIO48H or CIO-DIO192).
Either double click on the board or hit enter.
5. The board's default settings are then displayed. The board's defaults are:

BASE ADDRESS: 300H (768 Decimal) Same as data sheet.
WAIT STATE: OFF.

6. You are now ready to install the board in your computer. Open your PC (after turning off the power) and install the board. After the board is installed and the computer is closed up, turn the power back on.

7. Run *InstaCal*TM again, and at the main menu select *Test*.

- a. Select the board you just installed
- b. Select **Internal Test**
- c. The internal control registers of the board will then be tested. If this test is successful, your board is installed correctly. If not, you likely have a base address conflict, or have the base address switch set incorrectly. Please refer to the next chapter for more information regarding selecting and setting the base address.
- d. If the **Internal Test** is completed successfully, you may want to check that the I/O pins are working correctly. To check this select **External Test** and follow the instruction provided. This will require you to use the shorting wires supplied with the board to short inputs to outputs for I/O testing.

$$\text{Attenuation} = \frac{R1 + R2}{R2}$$

$$2 = \frac{10K + 10K}{10K}$$

$$R1 = (A - 1) * R2$$

The variable Attenuation is the proportional difference between the signal voltage max and the full scale of the analog input.

For example, if the signal varies between 0 and 20 volts and you wish to measure that with an analog input with a full scale range of 0 to 10 volts, the Attenuation is 2:1 or just 2.

For a given attenuation, pick a handy resistor and call it R2, then use this formula to calculate R1.

Digital inputs also make use of voltage dividers, for example, if you wish to measure a digital signal that is at 0 volts when off and 24 volts when on, you cannot connect that directly to the CIO-DIO digital inputs. The voltage must be dropped to 5 volts max when on. The Attenuation is 24:5 or 4.8. Use the equation above to find an appropriate R1 if R2 is 1K. Remember that a TTL input is 'on' when the input voltage is greater than 2.5 volts.

IMPORTANT NOTE: *The resistors, R1 and R2, are going to dissipate all the power in the divider circuit according to the equation Current = Voltage / Resistance. The higher the value of the resistance (R1 + R2) the less power dissipated by the divider circuit. Here is a simple rule:*

For Attenuation of 5:1 or less, no resistor should be less than 10K.

For Attenuation of greater than 5:1, no resistor should be less than 1K.

The CIO-TERMINAL has the circuitry on board to create custom voltage dividers. The CIO-TERMINAL is a 16" by 4" screw terminal board with two 37 pin D type connectors and 56 screw terminals (12 - 22 AWG). Designed for table top, wall or rack mounting, the board provides prototype, divider circuit, filter circuit and pull-up resistor positions which you may complete with the proper value components for your application.

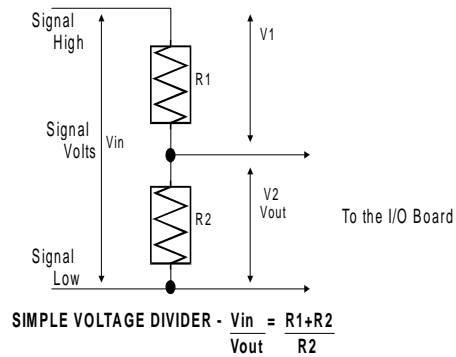
Voltage = Current * Resistance (commonly $V=IR$)

and Kirkoff's voltage law which states,

The sum of the voltage drops around a circuit will be equal to the voltage drop for the entire circuit.

Implied in the above is that any variation in the voltage drop for the circuit as a whole will have a *proportional* variation in all the voltage drops in the circuit.

A voltage divider takes advantage of the fact that the voltage across one of the resistors in a circuit is proportional to the voltage across the total resistance in the circuit.



The trick to using a voltage divider is to choose two resistors with the proper proportions relative to the full scale of the digital input and the maximum signal voltage.

The phenomena of dropping the voltage proportionally is often called attenuation. The formula for attenuation is:

OPERATION

INSTALLATION

The CIO-DIO48 has two 82C55 parallel interface chips and a 50 pin connector. Each 82C55 controls 24 CMOS TTL digital I/O pins. Within each 82C55, the digital I/O lines may be programmed as groups of 8,8 & 8 or 8,8 & 4,4). Each group may be input or output.

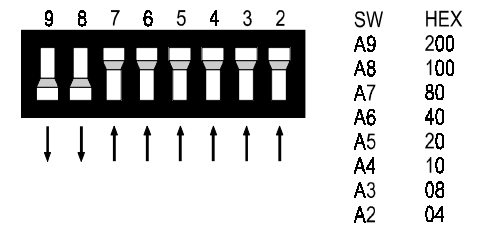
The CIO-DIO96 is exactly two CIO-DIO48 circuits on a single board.

The CIO-DIO192 is exactly 4 CIO-DIO48 circuits on a single board. All three boards share in common a base address switch, wait state jumper and 50 pin connector(s)

BASE ADDRESS

InstaCAL will help you select and set the board's base address. *InstaCAL* allows you to choose a desired base address and adjusts the base address if necessary to place it on an 8 bit boundary, CIO-DIO48, 16 bit boundary, CIO-DIO96 or 32 bit boundary, CIO-DIO192

The CIO-DIO employs the PC bus for power, communications and data transfer. As such it draws power from the PC, monitors the address lines and control signals and responds to its I/O address, and it receives and places data on the 8 data lines.



BASE ADDRESS SWITCH - Address 300H shown here.

The BASE address is the most important user selectable bus related feature of the CIO-DIO. The base address is the location that software writes to and reads from when communicating with the CIO-DIO.

The base address switch is the means for setting the base address. Each switch position corresponds to one of the PC bus address lines. By placing the switch down, the CIO-DIO address decode logic is instructed to respond to that address bit.

A complete address is constructed by calculating the HEX or decimal number which corresponds to all the address bits the CIO-DIO has been instructed to respond to. For example, shown to the right are address 9 and 8 DOWN, all others UP.

Address 9 = 200H (512D) and address 8 = 100H (256D), when added together they equal 300H (768D).

NOTE

DO NOT PAY ATTENTION TO THE NUMBERS PRINTED ON THE SWITCH. LOOK AT THE NUMBERS PRINTED IN WHITE ON THE BOARD!

Certain addresses are used by the PC, others are free and may be used by the CIO-DIO and other expansion boards. We recommend BASE = 300H (768D) be tried first.

HEX RANGE	FUNCTION	HEX RANGE	FUNCTION
000-00F	8237 DMA #1	2C0-2CF	EGA
020-021	8259 PIC #1	2D0-2DF	EGA
040-043	8253 TIMER	2E0-2E7	GPIB (AT)
060-063	82C55 PPI (XT)	2E8-2EF	SERIAL PORT
060-064	8742 CONTROLLER (AT)	2F8-2FF	SERIAL PORT
070-071	CMOS RAM & NMI MASK (AT)	300-30F	PROTOTYPE CARD
080-08F	DMA PAGE RESISTERS	310-31F	PROTOTYPE CARD
0A0-0A1	8259 PIC #2 (AT)	320-32F	HARD DISK (XT)
0A0-0AF	NMI MASK	378-37F	PARALLEL PRINTER
0C0-0DF	8237 #2 (AT)	380-38F	SDLC
0FF-0FF	80287 NUMERIC CO-P (AT)	3A0-3AF	SDLC
1F0-1FF	HARD DISK (AT)	3B0-3BB	MDA
200-20F	GAME CONTROL	3BC-3BF	PARALLEL PRINTER
210-21F	EXPANSION UNIT (XT)	3C0-3CF	EGA
238-23B	BUS MOUSE	3D0-3DF	CGA
23C-23F	ALT BUS MOUSE	3E8-3EF	SERIAL PORT
270-27F	PARALLEL PRINTER	3F0-3F7	FLOPPY DISK
2B0-2BF	EGA	3F8-3FF	SERIAL PORT

UNCONNECTED INPUTS FLOAT

Keep in mind that unconnected inputs float. If you are using a DIO board for input, and have unconnected inputs, ignore the data from those lines.

In other words, if you connect bit A0 and not bit A1, do not be surprised if A1 stays low, stays high or tracks A0... It is unconnected and so is not specified. The 82C55 is not malfunctioning. In the absence of a pull-up/down resistor, any input to a CIO-DIO which is unconnected is unspecified.

You do not have to tie input lines, and unconnected lines will not affect the performance of connected lines. Just make sure that you mask out any unconnected bits in software.

TTL TO SOLID STATE RELAYS

Many applications require digital outputs to switch AC and DC voltage motors on and off and to monitor AC and DC voltages. These AC and high DC voltages cannot be controlled or read directly by the TTL digital lines of a CIO-DIO.

Solid State Relays, allow control and monitoring of AC and high DC voltages and provide 750V isolation. Solid State Relays (SSRs) are the recommended method of interfacing to AC and high DC signals.

The most convenient way to use solid state relays and a CIO-DIO board is to purchase a Solid State Relay Rack. A SSR Rack is a circuit board with output buffer chips which are powerful enough to switch the SSR and sockets to plug SSRs into.

SSR Racks are available from most manufacturers of SSRs.

If you only want to drive one or two SSRs, all you need is a 74LS244 output buffer chip between the 82C55 output and the SSR. Of course the SSR will need a 5 volt power source as well.

VOLTAGE DIVIDERS

If you wish to measure a signal which varies over a range greater than the input range of a digital input, a voltage divider can drop the voltage of the input signal to the level the digital input can measure.

A voltage divider takes advantage of Ohm's law, which states,

If the inputs of the device you are controlling are left to float, they may float up or down. Which way they float is dependent on the characteristics of the circuit and the electrical environment; and unpredictable! This is why it often appears that the 82C55 has gone 'high' after power up. The result is that your controlled device gets turned on!

That is why you need pull up/down resistors.

Shown here is one 82C55 digital output with a pull-up resistor attached.

If the 82C55 is reset and enters high impedance input, the line is pulled high. At that point, both the 82C55 AND the device being controlled will sense a high signal.

If the 82C55 is in output mode, the 82C55 has more than enough power to override the pull-up resistor's high signal and drive the line to 0 volts. If the 82C55 asserts a high signal, the pull up resistor guarantees that the line goes to +5V.

Of course, a pull-down resistor accomplishes the same task except that the line is pulled low when the 82C55 is reset. The 82C55 has more than enough power to drive the line high.

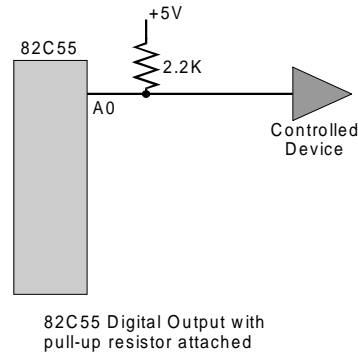
The CIO-DIO boards are equipped with positions for pull-up/down resistors Single Inline Packages (SIPs). The positions are marked A, B and C and are located beside the 82C55.

A 2.2K ohm, 8 resistor SIP is made of 8, 2.2K resistors all connected on one side to a common point and on the other, to a pin protruding from the SIP. The common line to which all resistor are connected also protrudes from the SIP. The common line is marked with a dot and is at one end of the SIP.

The SIP may be installed as pull-up or pull-down. At each location, A, B & C there are 10 holes in a line. One end of the line is +5V, the other end is GND. They are so marked. The 8 holes in the middle are connected to the 8 lines of the port, A, B, or C.

Install and solder the SIP in place.

A resistor value of 2.2K is recommended. Use other values only if you have calculated the necessity of doing so.



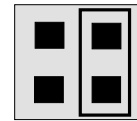
The CIO-DIO BASE switch may be set for address in the range of 000-3F0 so it should not be hard to find a free address area for you CIO-DIO. Once again, if you are not using IBM prototyping cards or some other board which occupies these addresses, then 300-31F HEX are free to use.

Addresses not specifically listed, such as 390-39F, are free.

WAIT STATE JUMPER

Some CIO-DIO boards have a wait state jumper which can enable an on-board wait state generator. A wait state is an extra delay injected into the processor's clock via the bus. This delay slows down the processor when the processor addresses the CIO-DIO board so that signals from slow devices (chips) will be valid.

The wait state generator on the CIO-DIO is only active when the CIO-DIO is being accessed. Your PC will not be slowed down in general by using the wait state.



ON OFF
WAIT STATE JUMPER BLOCK

Because all PC expansion board buses are slowed to either 8MHz or 10MHz, the wait state will generally not be required.

If you experience sporadic errors from the 82C55 digital I/O chip (reset, port direction swaps) you might try enabling the wait state generator.

INSTALLING THE CIO-DIO IN THE COMPUTER

Turn the power off.

Remove the cover of your computer. Please be careful not to dislodge any of the cables installed on the boards in your computer as you slide the cover off.

Locate an empty expansion slot in your computer.

Push the board firmly down into the expansion bus connector. If it is not seated fully it may fail to work and could short circuit the PC bus power onto a PC bus signal. This could damage the motherboard in your PC as well as the CIO-DIO.

CABLING TO THE DIO CONNECTOR

The CIO-DIO48 connector is accessible through the PC/AT expansion bracket. The connector is a standard 50 pin male header connector. A mating female connector may be purchased at Radio Shack or other electronic supply outlets.

SIGNAL CONNECTION - CIO-DIO48

All the digital outputs and inputs on the CIO-DIO48 connector are CMOS/TTL. TTL is an electronics industry term, short for Transistor-Transistor Logic, which describes a standard for digital signals which are either at 0V or 5V.

Under normal operating conditions, the voltages on the 82C55 pins range from 0 to 0.45 volts for the low state to between 2.4 to 5.0 volts for the high state. At a voltage of 0.45 volts the 82C55 can safely sink 2.5 mA. At a voltage of 2.4 volts the 82C55 can source 2.5 mA.

The voltages and currents associated with external devices range from less than a hundred mA at a few volts for a small flash light bulb to 50 Amps at 220 volts for a large electric range. Attempting to connect either of these devices directly to the CIO-DIO would destroy the I/O chip.

In addition to voltage and load matching, digital signal sources often need to be debounced. A complete discussion of digital interfacing will be found in the section on Interface Electronics in this manual.

IMPORTANT NOTE

The 82C55 digital I/O chip initializes all ports as inputs on power up and reset. A TTL input is a high impedance input. If you connect another TTL input device to the 82C55 it will probably be turned ON every time the 82C55 is reset, or, it might be turned OFF instead. Remember, and 82C55 which is reset is in INPUT mode.

To safeguard against unwanted signal levels, all devices being controlled by an 82C55 should be tied low (or high, as required) by a resistor.

You will find positions for pull up and pull down resistor packs on your CIO-DIO board. To implement these, please turn to the application note on pull up/down resistors.

ELECTRONICS AND INTERFACING

This short, simple introduction to the electronics most often needed by digital I/O board users covers a few key concepts. They are:

- Pull up/down resistors
- Transistors.
- Power MOSFETs
- Solid State Relays
- Voltage dividers.
- Low pass filters for digital inputs.
- Noise; sources and solutions.

IMPORTANT NOTE

It cannot be stated often enough to those unfamiliar with the 82C55. WHENEVER THE 82C55 IS POWERED ON OR RESET, ALL PINS ARE SET TO HIGH IMPEDANCE INPUT.

The implication of this fact is that if you have output devices such as solid state relays, they may be switched on whenever the computer is powered on or reset. To prevent unwanted switching and to drive all outputs to a known state after power on or reset, pull all pins either high or low through a 2.2K ohm resistor.

To install pull up/down resistor packs, see the application note.

PULL UP & PULL DOWN RESISTORS

This discussion deals with pull up/down resistors and 82C55 digital I/O chips on CIO-DIO boards.

Whenever the 82C55 is powered on or reset, the control register is set to a known state. That state is mode 0, all ports input.

When used as an output device to control other TTL input devices, the 82C55 applies a voltage level of 0V for low and 2.5V-5V for high. It is the output voltage level of the 82C55 that the device being controlled responds to.

DIGITAL I/O

TTL LEVEL DIRECT TO/FROM 82C55

82C55 output high	3.0 V min @ -2.5Ma
82C55 output low	0.4 V max @ 2.5 mA
82C55 input high	2.0 V min, 7 V max
82C55 input low	-0.5 V min, 0.8 V max
82C55 drive capability	5 LSTTL loads

HIGH DRIVE DIO48H

Output High	2.0V min @ -15mA
Output Low	0.55V max @ 64mA
Input High	2.0V min, 7.0V max
Input Low	0.8V max, -0.5V min

ENVIRONMENTAL

Operating Temperature	0 - 50 deg C
Storage Temperature	-20 to 70 deg C
Humidity	0 to 90% non-condensing
Weight	5 oz

UNCONNECTED INPUTS FLOAT

Keep in mind that unconnected inputs float. If you are using a DIO board for input, and have unconnected inputs, ignore the data from those lines.

In other words, if you connect bit A0 and not bit A1, do not be surprised if A1 stays low, stays high or tracks A0... It is unconnected and so is not specified. The 82C55 is not malfunctioning. In the absence of a pull-up/down resistor, any input to a CIO-DIO which is unconnected is unspecified.

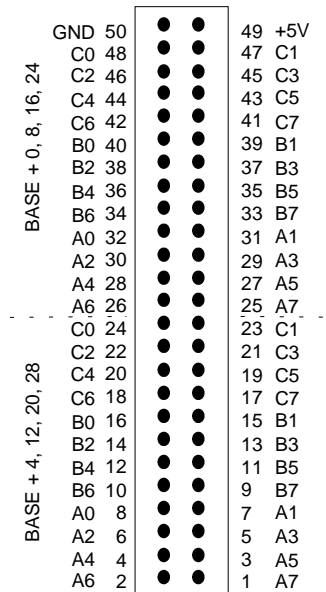
You do not have to tie input lines, and unconnected lines will not affect the performance of connected lines. Just make sure that you mask out any unconnected bits in software.

CONNECTOR DIAGRAM

The I/O connector for each of these boards is a 50 pin header connector accessible from the rear of the PC through the expansion backplate. The signals available are direct connections to an 82C55 digital I/O chip.

The connector accepts female 50 pin header connectors, such as those on the C50FF-2, 2 foot cable with connectors.

If frequent changes to signal connections or signal conditioning is required, please refer to the information on the CIO-TERM100, CIO-SPADE50 and CIO-MINI50 screw terminal boards.



ARCHITECTURE

SPECIFICATIONS

82C55 CONTROL & DATA REGISTERS

Each CIO-DIO is composed of 82C55 parallel I/O chips. Each chip contains 3 data and one control register occupying 4 consecutive I/O locations. The number of I/O locations occupied by a CIO-DIO board is equal to 4 times the number of 82C55 chips on the board.

The first address, or BASE ADDRESS, is determined by setting a bank of switches on the board.

A register is easy to read and write to.

The register descriptions follow the format shown below:

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Where the numbers along the top row are the bit positions within the 8 bit byte and the numbers and symbols in the bottom row are the functions associated with that bit.

To write to or read from a register in decimal or HEX, the following weights apply:

BIT POSITION	DECIMAL VALUE	HEX VALUE
0	1	1
1	2	2
2	4	4
3	8	8
4	16	10
5	32	20
6	64	40
7	128	80

To write a control word or data to a register, the individual bits must be set to 0 or 1 then combined to form a Byte. Data read from registers must be analyzed to determine which bits are on or off.

POWER CONSUMPTION

CIO-DIO48

+5V Supply	150 mA typical / 220 mA max.
+12V Supply	None.
-12V Supply	None.

CIO-DIO48H

+5V Supply	700 mA typical / 800 mA max.
+12V Supply	None.
-12V Supply	None.

CIO-DIO96

+5V Supply	190 mA typical / 320 mA max.
+12V Supply	None.
-12V Supply	None.

CIO-DIO192

+5V Supply	380 mA typical / 600 mA max.
+12V Supply	None.
-12V Supply	None.

NOTE

Additional power will be drawn by user's connections to the power pins accessible on CIO-DIO connectors.

The two groups of ports, group A and group B, may be independently programmed in one of several modes. The most commonly used mode is mode 0, input / output mode. The codes for programming the 82C55 in this mode are shown below. D7 is always 1 and D6, D5 & D2 are always 0.

D4	D3	D1	D0	HEX	DEC	A	CU	B	CL
0	0	0	0	80	128	OUT	OUT	OUT	OUT
0	0	0	1	81	129	OUT	OUT	OUT	IN
0	0	1	0	82	130	OUT	OUT	IN	OUT
0	0	1	1	83	131	OUT	OUT	IN	IN
0	1	0	0	88	136	OUT	IN	OUT	OUT
0	1	0	1	89	137	OUT	IN	OUT	IN
0	1	1	0	8A	138	OUT	IN	IN	OUT
0	1	1	1	8B	139	OUT	IN	IN	IN
1	0	0	0	90	144	IN	OUT	OUT	OUT
1	0	0	1	91	145	IN	OUT	OUT	IN
1	0	1	0	92	146	IN	OUT	IN	OUT
1	0	1	1	93	147	IN	OUT	IN	IN
1	1	0	0	98	152	IN	IN	OUT	OUT
1	1	0	1	99	153	IN	IN	OUT	IN
1	1	1	0	9A	154	IN	IN	IN	OUT
1	1	1	1	9B	155	IN	IN	IN	IN

The method of programming required to set/read bits from bytes is beyond the scope of this manual. It will be covered in most Introduction To Programming books, available from a bookstore.

In summary form, the registers and their function are listed on the following table. Within each register are 8 bits which may constitute a byte of data or 8 individual bit set/read functions.

ADDRESS	READ FUNCTION	WRITE FUNCTION
BASE + 0	Port A Input of 82C55	Port A Output
BASE + 1	Port B Input	Port B Output
BASE + 2	Port C Input	Port C Output
BASE + 3	None. No read back on 82C55	Configure 82C55
BASE + 4	Port A Input of 82C55	Port A Output
BASE + 5	Port B Input	Port B Output
BASE + 6	Port C Input	Port C Output
BASE + 7	None. no read back on 82C55	Configure 82C55
	ADDITIONAL CIO-DIO96 & 192 ONLY	
BASE + 8	Port A Input of 82C55	Port A Output
BASE + 9	Port B Input	Port B Output
BASE + 10	Port C Input	Port C Output
BASE + 11	None. No read back on 82C55	Configure 82C55
BASE + 12	Port A Input of 82C55	Port A Output
BASE + 13	Port B Input	Port B Output
BASE + 14	Port C Input	Port C Output
BASE + 15	None. no read back on 82C55	Configure 82C55
	ADDITIONAL CIO-DIO 192 ONLY	
BASE + 16	Port A Input of 82C55	Port A Output
BASE + 17	Port B Input	Port B Output
BASE + 18	Port C Input	Port C Output
BASE + 19	None. No read back on 82C55	Configure 82C55
BASE + 20	Port A Input of 82C55	Port A Output
BASE + 21	Port B Input	Port B Output
BASE + 22	Port C Input	Port C Output
BASE + 23	None. no read back on 82C55	Configure 82C55
BASE + 24	Port A Input of 82C55	Port A Output
BASE + 25	Port B Input	Port B Output
BASE + 26	Port C Input	Port C Output
BASE + 27	None. No read back on 82C55	Configure 82C55
BASE + 28	Port A Input of 82C55	Port A Output
BASE + 29	Port B Input	Port B Output
BASE + 30	Port C Input	Port C Output
BASE + 31	None. No read back on 82C55	Configure 82C55

82C55 DIGITAL I/O REGISTERS

PORT A DATA

BASE ADDRESS +0

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

PORT B DATA

BASE ADDRESS +1

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

Ports A & B may be programmed as input or output. Each is written to and read from in Bytes, although for control and monitoring purposes the individual bits are more interesting.

Bit set/reset and bit read functions require that unwanted bits be masked out of reads and ORed into writes.

PORT C DATA

BASE ADDRESS +2 (8-bit mode)

7	6	5	4	3	2	1	0
C8	C7	C6	C5	C4	C3	C2	C1
CH4	CH3	CH2	CH1	CL4	CL3	CL2	CL1

Port C may be used as one 8 bit port of either input or output, or it may be split into two 4 bit ports which may be independently input or output.

PORT C DATA

BASE ADDRESS +2 (4-bit mode)

7	6	5	4	3	2	1	0
C8	C7	C6	C5	C4	C3	C2	C1
CH4	CH3	CH2	CH1	CL4	CL3	CL2	CL1

The notation for the upper 4 bit port is PCH3-PCH0, and for the lower, PCL3-PCL0.

Although it may be split, every read and write to port C carries 8 bits of data so unwanted information must be ANDed out of reads, and writes must be ORed with the current status of the other port.

OUTPUT PORTS

In 82C55 mode 0 configuration, ports configured for output hold the output data written. The output byte may be read back by reading a port configured for output.

INPUT PORTS

In 82C55 mode 0 configuration, ports configured for input read the state of the input lines at the moment the read is executed, transitions are not latched.

For information on modes 1 (strobed I/O) and 2 (bi-directional strobed I/O), you will need to acquire an Intel or AMD data book and see the 82C55 data sheet.

82C55 CONTROL REGISTER

BASE ADDRESS +3

7	6	5	4	3	2	1	0
MS	M3	M2	A	CU	M1	B	CL
Group A				Group B			

The 82C55 may be programmed to operate in Input/ Output (mode 0), Strobed Input/ Output (mode 1) or Bi-Directional Bus (mode 2).

Included here is information on programming the 82C55 in mode 0. Those wishing to use the 82C55 in modes 1 or 2, must procure a data book from Intel Corporation Literature Department.

When the PC is powered up or RESET, the 82C55 is reset. This places all 24 lines in Input mode and no further programming is needed to use the 24 lines as TTL inputs.

To program the 82C55 for other modes, the following control code byte must be assembled into an 8 bit byte.

M3	M2	Group A Function		
0	0	Mode 0	Input / Output	
0	1	Mode 1	Strobed Input / Output	
1	X	Mode 2	Bi-Directional	
A	B	CL	CH	Independent Function
1	1	1	1	Input
0	0	0	0	Output

M1 = 0 is mode 0 for group B. Input / Output

M1 = 1 is mode 1 for group B. Strobed Input / Output

The Ports A, B, C High and C Low may be independently programmed for input or output.