User's Guide

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Universal Digital I/O Interface
24, 48 and 168 Channel

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FUNCTIONAL DESCRIPTION

The Digital I/O Interface provides a general purpose TTL interface for the IBM PC/XT and AT Computers, (and true compatibles). The I/O lines are provided by industry standard 8255-5 PPI IC's, each grouped into three ports of (8) lines each. See Figures 1, 2 and 3. These ports may be configured by software as either inputs (read) or outputs (write).

The Digital I/O Interface may also be used with industry standard optically isolated I/O modules. (OPTO-22, GORDOS, etc.) This enables the user to sense and control a variety of voltage levels, (110 VAC, 220 VAC, 24 VDC, etc.) from the computer.

Also, on-board are 8253 Counter Timer Chips (CTC's), which each supply 16-bit counter/timers. A 1 MHz TTL Oscillator is on-board to provide a time base for any of the counters on the first 8253. *(CTC's and Oscillators not supplied on 24 Channel board)*

A complete description of the 8255A Programmable Peripheral Interface can be found in Appendix A, and the 8253 Counter/Timer in Appendix B.

Performance Note:

Some digital I/O boards on the market employ a address/data multiplexing strategy. This is at the sacrifice of throughput. Our boards do not use multiplexing! In the time it takes to do one assembly instruction (OUT), 8 of the outputs are updated. Included on the disk provided with the board, is an program named "BENCHMAR.EXE". This is an access averaging program to give the I/O updating speed for the specific CPU in question. To determine the average throughput of a machine, insert the disk in drive A: and type BENCHMAR <ENTER>. The program will time 50,000 accesses and print the speed on the monitor.

SPECIFICATIONS 24 Channel Board

Environmental:

Storage Temperature	-40 to +100 deg. C
Operating Temperature	0-70 deg. C
Humidity	0 to 90% non-condensing
Size	Half Slot
Bus Loading (Max)	400ma @ +5 VDC

Digital I/O: (8255A-5 PPI + 74LS245 Buffering)

Quantity	24
Input logic low voltage	-0.5 V min. to 0.8 V max.
Input logic high voltage	2.0 V min. to 5.0 V max.
Input load current	-10 uA min. to +10 uA max.
Output low voltage	0.45 V max.
Output high voltage	2.4 V min.
Output Source Current	15ma
Output Sink Current	24ma
I/O Connectors	One 26-pin Male header One 37-pin Male D-Sub One 50-pin Male header

Note: Digital lines are TTL/DTL compatible. The drivers used are 74LS245 Bus Transceivers.

This board does not include Counter/Timers

SPECIFICATIONS 48 Channel Board

Environmental:

Storage Temperature	-40 to +100 deg. C
Operating Temperature	0-70 deg. C
Humidity	0 to 90% non-condensing
Size	Half Slot
Bus Loading (Max)	600ma @ +5 VDC

Digital I/O: (8255A-5 PPI)

Quantity	48
Input logic low voltage	-0.5 V min. to 0.8 V max.
Input logic high voltage	2.0 V min. to 5.0 V max.
Input load current	-10 uA min. to +10 uA max.
Output low voltage	0.45 V max.
Output high voltage	2.4 V min.
I/O Connectors	Two 26-pin Male headers

Note: Digital lines are TTL/DTL compatible and will drive 1 standard (74 type) TTL Load or 4 (74LS type) LSTTL loads. *A 10Kohm resistor to +5 VDC is supplied on each digital I/O line providing CMOS compatibility.*

Counter I/O: (8253-5 CTC)

Quantity	6
Resolution	16 bits
Frequency	DC to 2.6 MHz
Input logic low voltage	-0.5 V min. to 0.8 V max.
Input logic high voltage	2.0 V min. to 5.0 V max.
Input load current	-10 uA min. to +10 uA max.
Output low voltage	0.45 V max.
Output high voltage	2.4 V min.
I/O Connectors	Two 16-pin Male headers

SPECIFICATIONS 168 Channel Board

Environmental:

Storage Temperature	-40 to +100 deg. C
Operating Temperature	0-70 deg. C
Humidity	0 to 90% non-condensing
Size	Full Slot
Bus Loading (Max)	600ma @ +5 VDC

Digital I/O: (8255A-5 PPI)

Quantity	168
Input logic low voltage	-0.5 V min. to 0.8 V max.
Input logic high voltage	2.0 V min. to 5.0 V max.
Input load current	-10 uA min. to +10 uA max.
Output low voltage	0.45 V max.
Output high voltage	2.4 V min.
I/O Connectors	Seven 26-pin Male headers

Note: Digital lines are TTL/DTL compatible and will drive 1 standard (74 type) TTL Load or 4 (74LS type) LSTTL loads. *A 10Kohm resistor to +5 VDC is supplied on each digital I/O line providing CMOS compatibility.*

Counter I/O: (8253-5 CTC)

Quantity	3
Resolution	16 bits
Frequency	DC to 2.6 MHz
Input logic low voltage	-0.5 V min. to 0.8 V max.
Input logic high voltage	2.0 V min. to 5.0 V max.
Input load current	-10 uA min. to +10 uA max.
Output low voltage	0.45 V max.
Output high voltage	2.4 V min.
I/O Connectors	One 16-pin Male header

HARDWARE INSTALLATION

There are two user-configurable parameters on the card; the BASE I/O address, and the Interrupt Request Number (IRQ). As shipped from the factory, the BASE address is 280H, and the IRQ number is 7. To get the system running rarely requires any jumper change. See Figures 1, 2 and 3 for a diagram of the default jumper positions. In case of difficulty, return the system to its default settings.

Note: If you need two or more Digital I/O cards in your system, we recommend the first card be addressed at the default (280H); and the second card be addressed at the next available address shown. By addressing the cards at consecutive addresses, any table driven software access is simplified.

No other card in the system may use the same Base Address or any of the addresses used by the board. Care must be taken that no address conflicts exist. Addresses 200H through 3FFH are available to plug in cards. The common assignments are found in Table 1.

COMMON BASE ADDRESS ASSIGNMENTS

Address Hex	Peripheral
200 - 20F	Game I/O
210 - 217	Expansion unit
220 - 24F	Reserved
250 - 277	Not used
278 - 27F	LPT2 (printer)
280 - 2EF	Not used
2F0 - 2F7	Reserved
2F8 - 2FF	COM2 (serial)
300 - 31F	Not used
320 - 32F	Hard Disk
330 - 377	Not Used
378 - 37F	LPT1
380 - 38C	SDLC communications
390 - 39F	Not Used
3A0 - 3A9	BYSYNC #1
3B0 - 3BF	Mono display w/ parallel
3C0 - 3CF	Reserved
3D0 - 3DF	Color graphics display
3E0 - 3EF	Reserved
3F0 - 3F7	5 1/4" Floppy controller
3F8 - 3FF	COM1

Table 1

Base Address Selection - 24 Channel Board

The entire card uses a block of 4 I/O addresses. All addresses within the 4 address block are fixed with respect to the base address. The base address is configured by switch positions 1 through 8 on the card. These switches are used to create a hexadecimal *Address*. See Figure 1 for the switch location, and their relative value. Note that if the switch is ON, the value is 0. All the possible base address settings are shown in Tables 2A through 2D.

POSSIBLE BASE ADDRESS SETTINGS

DIP Switch Position								Base Address Selection (HEX)
3	4	5	6	7	8	9	10	
ON	ON	ON	ON	ON	ON	ON	OFF	200
OFF	ON	ON	ON	ON	ON	ON	OFF	204
ON	OFF	ON	ON	ON	ON	ON	OFF	208
OFF	OFF	ON	ON	ON	ON	ON	OFF	20C
ON	ON	OFF	ON	ON	ON	ON	OFF	210
OFF	ON	OFF	ON	ON	ON	ON	OFF	214
ON	OFF	OFF	ON	ON	ON	ON	OFF	218
OFF	OFF	OFF	ON	ON	ON	ON	OFF	21C
ON	ON	ON	OFF	ON	ON	ON	OFF	220
OFF	ON	ON	OFF	ON	ON	ON	OFF	224
ON	OFF	ON	OFF	ON	ON	ON	OFF	228
OFF	OFF	ON	OFF	ON	ON	ON	OFF	22C
ON	ON	OFF	OFF	ON	ON	ON	OFF	230
OFF	ON	OFF	OFF	ON	ON	ON	OFF	234
ON	OFF	OFF	OFF	ON	ON	ON	OFF	238
OFF	OFF	OFF	OFF	ON	ON	ON	OFF	23C
ON	ON	ON	ON	OFF	ON	ON	OFF	240
OFF	ON	ON	ON	OFF	ON	ON	OFF	244
ON	OFF	ON	ON	OFF	ON	ON	OFF	248
OFF	OFF	ON	ON	OFF	ON	ON	OFF	24C
ON	ON	OFF	ON	OFF	ON	ON	OFF	250
OFF	ON	OFF	ON	OFF	ON	ON	OFF	254
ON	OFF	OFF	ON	OFF	ON	ON	OFF	258
OFF	OFF	OFF	ON	OFF	ON	ON	OFF	25C
ON	ON	ON	OFF	OFF	ON	ON	OFF	260
OFF	ON	ON	OFF	OFF	ON	ON	OFF	264
ON	OFF	ON	OFF	OFF	ON	ON	OFF	268
OFF	OFF	ON	OFF	OFF	ON	ON	OFF	26C
ON	ON	OFF	OFF	OFF	ON	ON	OFF	270
OFF	ON	OFF	OFF	OFF	ON	ON	OFF	274
ON	OFF	OFF	OFF	OFF	ON	ON	OFF	278
OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	27C

Table 2A

Base Address Selection - 24 Channel Board (continued)

POSSIBLE BASE ADDRESS SETTINGS

DIP Switch Position								Base Address Selection (HEX)
3	4	5	6	7	8	9	10	
ON	ON	ON	ON	ON	OFF	ON	OFF	280
OFF	ON	ON	ON	ON	OFF	ON	OFF	284
ON	OFF	ON	ON	ON	OFF	ON	OFF	288
OFF	OFF	ON	ON	ON	OFF	ON	OFF	28C
ON	ON	OFF	ON	ON	OFF	ON	OFF	290
OFF	ON	OFF	ON	ON	OFF	ON	OFF	294
ON	OFF	OFF	ON	ON	OFF	ON	OFF	298
OFF	OFF	OFF	ON	ON	OFF	ON	OFF	29C
ON	ON	ON	OFF	ON	OFF	ON	OFF	2A0
OFF	ON	ON	OFF	ON	OFF	ON	OFF	2A4
ON	OFF	ON	OFF	ON	OFF	ON	OFF	2A8
OFF	OFF	ON	OFF	ON	OFF	ON	OFF	2AC
ON	ON	OFF	OFF	ON	OFF	ON	OFF	2B0
OFF	ON	OFF	OFF	ON	OFF	ON	OFF	2B4
ON	OFF	OFF	OFF	ON	OFF	ON	OFF	2B8
OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	2BC
ON	ON	ON	ON	OFF	OFF	ON	OFF	2C0
OFF	ON	ON	ON	OFF	OFF	ON	OFF	2C4
ON	OFF	ON	ON	OFF	OFF	ON	OFF	2C8
OFF	OFF	ON	ON	OFF	OFF	ON	OFF	2CC
ON	ON	OFF	ON	OFF	OFF	ON	OFF	2D0
OFF	ON	OFF	ON	OFF	OFF	ON	OFF	2D4
ON	OFF	OFF	ON	OFF	OFF	ON	OFF	2D8
OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	2DC
ON	ON	ON	OFF	OFF	OFF	ON	OFF	2E0
OFF	ON	ON	OFF	OFF	OFF	ON	OFF	2E4
ON	OFF	ON	OFF	OFF	OFF	ON	OFF	2E8
OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	2EC
ON	ON	OFF	OFF	OFF	OFF	ON	OFF	2F0
OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	2F4
ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	2F8
OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	2FC

Table 2B

Base Address Selection - 24 Channel Board (continued)

POSSIBLE BASE ADDRESS SETTINGS

DIP Switch Position								Base Address Selection (HEX)
3	4	5	6	7	8	9	10	
ON	ON	ON	ON	ON	ON	OFF	OFF	300
OFF	ON	ON	ON	ON	ON	OFF	OFF	304
ON	OFF	ON	ON	ON	ON	OFF	OFF	308
OFF	OFF	ON	ON	ON	ON	OFF	OFF	30C
ON	ON	OFF	ON	ON	ON	OFF	OFF	310
OFF	ON	OFF	ON	ON	ON	OFF	OFF	314
ON	OFF	OFF	ON	ON	ON	OFF	OFF	318
OFF	OFF	OFF	ON	ON	ON	OFF	OFF	31C
ON	ON	ON	OFF	ON	ON	OFF	OFF	320
OFF	ON	ON	OFF	ON	ON	OFF	OFF	324
ON	OFF	ON	OFF	ON	ON	OFF	OFF	328
OFF	OFF	ON	OFF	ON	ON	OFF	OFF	32C
ON	ON	OFF	OFF	ON	ON	OFF	OFF	330
OFF	ON	OFF	OFF	ON	ON	OFF	OFF	334
ON	OFF	OFF	OFF	ON	ON	OFF	OFF	338
OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	33C
ON	ON	ON	ON	OFF	ON	OFF	OFF	340
OFF	ON	ON	ON	OFF	ON	OFF	OFF	344
ON	OFF	ON	ON	OFF	ON	OFF	OFF	348
OFF	OFF	ON	ON	OFF	ON	OFF	OFF	34C
ON	ON	OFF	ON	OFF	ON	OFF	OFF	350
OFF	ON	OFF	ON	OFF	ON	OFF	OFF	354
ON	OFF	OFF	ON	OFF	ON	OFF	OFF	358
OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	35C
ON	ON	ON	OFF	OFF	ON	OFF	OFF	360
OFF	ON	ON	OFF	OFF	ON	OFF	OFF	364
ON	OFF	ON	OFF	OFF	ON	OFF	OFF	368
OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	36C
ON	ON	OFF	OFF	OFF	ON	OFF	OFF	370
OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	374
ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	378
OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	37C

Table 2C

Base Address Selection - 24 Channel Board (continued)

POSSIBLE BASE ADDRESS SETTINGS

DIP Switch Position								Base Address Selection (HEX)
3	4	5	6	7	8	9	10	
ON	ON	ON	ON	ON	OFF	OFF	OFF	380
OFF	ON	ON	ON	ON	OFF	OFF	OFF	384
ON	OFF	ON	ON	ON	OFF	OFF	OFF	388
OFF	OFF	ON	ON	ON	OFF	OFF	OFF	38C
ON	ON	OFF	ON	ON	OFF	OFF	OFF	390
OFF	ON	OFF	ON	ON	OFF	OFF	OFF	394
ON	OFF	OFF	ON	ON	OFF	OFF	OFF	398
OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	39C
ON	ON	ON	OFF	ON	OFF	OFF	OFF	3A0
OFF	ON	ON	OFF	ON	OFF	OFF	OFF	3A4
ON	OFF	ON	OFF	ON	OFF	OFF	OFF	3A8
OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	3AC
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	3B0
OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	3B4
ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	3B8
OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	3BC
ON	ON	ON	ON	OFF	OFF	OFF	OFF	3C0
OFF	ON	ON	ON	OFF	OFF	OFF	OFF	3C4
ON	OFF	ON	ON	OFF	OFF	OFF	OFF	3C8
OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	3CC
ON	ON	OFF	ON	OFF	OFF	OFF	OFF	3D0
OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	3D4
ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	3D8
OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	3DC
ON	ON	ON	OFF	OFF	OFF	OFF	OFF	3E0
OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	3E4
ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	3E8
OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	3EC
ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	3F0
OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	3F4
ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3F8
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3FC

Table 2D

Base Address Selection - 48 Channel Board

The entire card uses a block of 16 I/O addresses. All addresses within the 16 address block are fixed with respect to the base address. The base address is configured by switch positions 5 through 10 on the card. These switches are used to create a hexadecimal *Address*. See Figure 2 for the switch location, and their relative value. Note that if the switch is ON, the value is 0. All the possible base address settings are shown in Table 3.

POSSIBLE BASE ADDRESS SETTINGS

DIP Switch Position						Base Address Selection (HEX)
5	6	7	8	9	10	
ON	ON	ON	ON	ON	OFF	200
OFF	ON	ON	ON	ON	OFF	210
ON	OFF	ON	ON	ON	OFF	220
OFF	OFF	ON	ON	ON	OFF	230
ON	ON	OFF	ON	ON	OFF	240
OFF	ON	OFF	ON	ON	OFF	250
ON	OFF	OFF	ON	ON	OFF	260
OFF	OFF	OFF	ON	ON	OFF	270
ON	ON	ON	OFF	ON	OFF	280
OFF	ON	ON	OFF	ON	OFF	290
ON	OFF	ON	OFF	ON	OFF	2A0
OFF	OFF	ON	OFF	ON	OFF	2B0
ON	ON	OFF	OFF	ON	OFF	2C0
OFF	ON	OFF	OFF	ON	OFF	2D0
ON	OFF	OFF	OFF	ON	OFF	2E0
OFF	OFF	OFF	OFF	ON	OFF	2F0
ON	ON	ON	ON	OFF	OFF	300
OFF	ON	ON	ON	OFF	OFF	310
ON	OFF	ON	ON	OFF	OFF	320
OFF	OFF	ON	ON	OFF	OFF	330
ON	ON	OFF	ON	OFF	OFF	340
OFF	ON	OFF	ON	OFF	OFF	350
ON	OFF	OFF	ON	OFF	OFF	360
OFF	OFF	OFF	ON	OFF	OFF	370
ON	ON	ON	OFF	OFF	OFF	380
OFF	ON	ON	OFF	OFF	OFF	390
ON	OFF	ON	OFF	OFF	OFF	3A0
OFF	OFF	ON	OFF	OFF	OFF	3B0
ON	ON	OFF	OFF	OFF	OFF	3C0
OFF	ON	OFF	OFF	OFF	OFF	3D0
ON	OFF	OFF	OFF	OFF	OFF	3E0
OFF	OFF	OFF	OFF	OFF	OFF	3F0

Table 3

Base Address Selection - 168 Channel Board

The entire card uses a block of 32 I/O addresses. All addresses within the 32 address block are fixed with respect to the base address. The base address is configured by switch positions 6 through 10 on the card. These switches are used to create a hexadecimal *Address*. See Figure 3 for the switch location, and their relative value. Note that if the switch is ON, the value is 0. All the possible base address settings are shown in Table 4.

POSSIBLE BASE ADDRESS SETTINGS

DIP Switch Position 6	7	8	9	10	Base Address Selection (HEX)
ON	ON	ON	ON	OFF	200
OFF	ON	ON	ON	OFF	220
ON	OFF	ON	ON	OFF	240
OFF	OFF	ON	ON	OFF	260
ON	ON	OFF	ON	OFF	280
OFF	ON	OFF	ON	OFF	2A0
ON	OFF	OFF	ON	OFF	2C0
OFF	OFF	OFF	ON	OFF	2E0
ON	ON	ON	OFF	OFF	300
OFF	ON	ON	OFF	OFF	320
ON	OFF	ON	OFF	OFF	340
OFF	OFF	ON	OFF	OFF	360
ON	ON	OFF	OFF	OFF	380
OFF	ON	OFF	OFF	OFF	3A0
ON	OFF	OFF	OFF	OFF	3C0
OFF	OFF	OFF	OFF	OFF	3E0

Table 4

Note: The 168 Channel board offers special addressing for '286 and '386 machines. This allows for upto 4 boards to occupy the same address space in the I/O page. To utilize this feature, move the jumpers from the "XT" position to the "AT" position. Now switches 4 and 5 will choose the *page* address desired. Switch 4 has a binary value of 800H and switch 5 a value of 1000H. Remember that an "OFF" switch is a "TRUE".

Example:	Switches 6 to 10 have address of:	280H
	Switch 4 is OFF	+ 800H
	Switch 5 is ON	+ 000H

	Board's BASE Address	A80H

Interrupt Request Selection - 24 Channel Board

The selected IRQ line is available on the 37 pin D-SUB connector. The line is passed through a 74LS125 Tri-State buffer. Therefore, the ENABLE line on the 37 pin D-SUB must be held low (to GND) for the IRQ to be passed through to the bus. Remember that interrupts are TRUE HIGH on the PC-Bus. Care must be taken that a proper Interrupt Service Routine is installed at the IBM interrupt vector address. If no routine is present, *unpredictable* results will occur.

Interrupt Request Selection - 48 and 168 Channel Boards

The OUT0 line from 8253 #1 (J2) may be connected to a PC BUS interrupt request line via an on-board jumper (See Figure 2 and 3). IRQ (interrupt request) lines 2, 3, 4, 5 and 7 are provided. See Table 3 for interrupt assignments. The selected interrupt will occur when OUT0 goes from low to high. This can be caused by either a time interval, or a terminal count on Counter 0. Care must be taken that a proper Interrupt Service Routine is installed at the IBM interrupt vector address. If no routine is present, *unpredictable* results will occur.

INTERRUPT REQUEST ASSIGNMENTS

Interrupt		Peripheral	
IRQ2	-	Reserved (Available on XT) (IRQ 9 on AT)	
IRQ3	-	COM2: or SDLC	*see note
IRQ4	-	COM1: or SDLC	*see note
IRQ5	-	Fixed Disk	
IRQ6	-	Floppy Disk	
IRQ7	-	Parallel Printer	*see note

Table 5

Note: Under a normal DOS environment, IRQ3, 4 and 7 are available even if the above devices are installed. If however, an *interrupt driven* software driver is installed for COM1, COM2, or the printer, the corresponding interrupt will no longer be available to other cards. Also, if the system is an "AT", IRQ2 is then rerouted to IRQ9. Therefore, additional software is required to use this configuration.

PROGRAMMING

Registers - 24 Channel Board

The card requires a block of 4 I/O register addresses. All communication with the card is accomplished within these 4 registers. See Table 4 for individual register assignments. Figure 1 may also be helpful to interpret the relationships between registers and devices.

I/O REGISTER ASSIGNMENTS

	Address	Function
8255 #1		
	BASE + 00H	JO, Port A
	BASE + 01	JO, Port B
	BASE + 02	JO, Port C
	BASE + 03	Control register

Table 6

Registers - 48 Channel Board

The card requires a block of 16 I/O register addresses. All communication with the card is accomplished within these 16 registers. Within the block of 16 addresses are 4 groups of four addresses. The four groups access the first 8255 PPI, the second 8255 PPI, the first 8253 CTC, and the second 8253 CTC respectively. See Table 4 for individual register assignments. Figure 2 may also be helpful to interpret the relationships between registers and devices.

I/O REGISTER ASSIGNMENTS

	Address	Function
8255 #1		
	BASE + 00H	J0, Port A
	BASE + 01	J0, Port B
	BASE + 02	J0, Port C
	BASE + 03	Control register
8255 #2		
	BASE + 04	J1, Port A
	BASE + 05	J1, Port B
	BASE + 06	J1, Port C
	BASE + 07	Control register
8253 #1		
	BASE + 08	J2, Counter 0
	BASE + 09	J2, Counter 1
	BASE + 0A	J2, Counter 2
	BASE + 0B	Control register
8253 #2		
	BASE + 0C	J3, Counter 0
	BASE + 0D	J3, Counter 1
	BASE + 0E	J3, Counter 2
	BASE + 0F	Control register

Table 7

Registers - 168 Channel Board

The card requires a block of 32 I/O register addresses. All communication with the card is accomplished within these 32 registers. Within the block of 32 addresses are 8 groups of four addresses. The eight groups access the first 8255 PPI, to the last 8255 PPI, and then the 8253 CTC. See Table 4 for individual register assignments. Figure 3 may also be helpful to interpret the relationships between registers and devices.

I/O REGISTER ASSIGNMENTS

	Address	Function
8255 #1		
	BASE + 00H	J0, Port A
	BASE + 01	J0, Port B
	BASE + 02	J0, Port C
	BASE + 03	Control register
8255 #2		
	BASE + 04	J1, Port A
	BASE + 05	J1, Port B
	BASE + 06	J1, Port C
	BASE + 07	Control register
8255 #3		
	BASE + 08	J2, Port A
	BASE + 09	J2, Port B
	BASE + 0a	J2, Port C
	BASE + 0b	Control register
8255 #4		
	BASE + 0c	J3, Port A
	BASE + 0d	J3, Port B
	BASE + 0e	J3, Port C
	BASE + 0f	Control register
8255 #5		
	BASE + 10	J4, Port A
	BASE + 11	J4, Port B
	BASE + 12	J4, Port C
	BASE + 13	Control register
8255 #6		
	BASE + 14	J5, Port A
	BASE + 15	J5, Port B
	BASE + 16	J5, Port C
	BASE + 17	Control register
8255 #7		
	BASE + 18	J6, Port A
	BASE + 19	J6, Port B
	BASE + 1a	J6, Port C
	BASE + 1b	Control register
8253 #1		
	BASE + 1c	J7, Counter 0
	BASE + 1d	J7, Counter 1
	BASE + 1e	J7, Counter 2
	BASE + 1f	Control register

Table 8

8255 PPI Initialization

Prior to any I/O activity, the 8255 PPI Control Register must be initialized. This is accomplished by writing an 8 bit control word to the 8255's Control Register address. Once this is done, the 24 I/O lines on the 8255 PPI may be accessed at any time by reading or writing to the appropriate port registers A, B, or C. Note that if +5 VDC power is lost, or the PC is reset, the Control Register must be reinitialized.

The 8255 PPI is capable of several modes of operation. The simplest and most common, Mode 0 - Basic I/O , will be discussed here. If the application requires one of the more complex modes, the user is referred to the 8255 PPI Data Sheet in Appendix A.

The *direction* of an I/O signal is termed "Input" for reading the signal or "Output" for writing the signal. Direction is assigned to eight lines at a time and are referred to as Port A (lines 0 - 7), Port B (lines 8-15), and Port C (lines 16-23). It is possible to "split" Port C into two 4 line ports (lines 16-19 and lines 20-23). The user is referred to 8255 PPI Data Sheet in Appendix A if this is required.

POSSIBLE 8255 MODE WORDS

HEX	DEC	PORT A	PORT B	PORT C
80	128	OUTPUT	OUTPUT	OUTPUT
82	130	OUTPUT	INPUT	OUTPUT
89	137	OUTPUT	OUTPUT	INPUT
8B	139	OUTPUT	INPUT	INPUT
90	144	INPUT	OUTPUT	OUTPUT
92	146	INPUT	INPUT	OUTPUT
99	153	INPUT	OUTPUT	INPUT
9B	155	INPUT	INPUT	INPUT

Table 9

Initialization Program Examples

An example of setting the *first* 8255 PPI lines 0-7 as "Inputs", lines 8-15 as "Outputs", and lines 16-23 and "Inputs" is as follows:

In "GWBASIC"

```
10 BASE = &H280              ' the dip switch setting on the card
20 OUT BASE + 3, &H99        '      write to the control register
```

In "Turbo Pascal"

```
const BASE = $280;           {the dip switch setting on the card}
 begin
  PORT[BASE + 3] := $99;          {write to the control register}
 end;
```

An example of setting the *second* 8255 PPI lines 0-7 as all "Inputs" is as follows:

In "GWBASIC"

```
10 BASE = &H280              ' the dip switch setting on the card
20 OUT BASE + 7, &H9B        '      write to the control register
```

In "Turbo Pascal"

```
const BASE = $280;           {the dip switch setting on the card}
 begin
  PORT[BASE + 7] := $9B;          {write to the control register}
 end;
```

8255 PPI Data Access (General)

Once the Control Register is set, the 8255 PPI is ready to perform digital I/O. Ports configured as "Outputs" are *write only*, and ports configured as "Inputs" are *read only*. In the case of the above configuration, 8255 PPI #1, Port A is set as "Inputs". Therefore, when reading Port A, the 8 bit data received is a representation of the voltage levels on PA0 through PA7. PA0 is the least significant bit and PA7 is the most significant bit. A TTL "Low" is represented by a 0 bit and a TTL "High" is represented by a 1 bit.

8255 PPI Data Access (Inputs)

For an example we will assume that PA0 through PA3 are at TTL "Low" levels and PA4 through PA7 are at TTL "High" levels. The following program could be used to read these levels:

In "GWBASIC"

```
  10 BASE = &H280           ' the dip switch setting on the card
  20 DAT  = INP(BASE + 0)   '                     read PORT A Data
```

In "Turbo Pascal"

```
  const BASE = $280;        {the dip switch setting on the card}
  var   DAT  : byte;
   begin
    DAT  := PORT[BASE + $00] {                     read PORT A Data}
   end;
```

The value of the variable DAT after this code is executed will be 240 decimal, or in binary 11110000. Note that the least significant 4 bits (PA0-PA3), are 0. This corresponds to TTL "Low" levels on these lines. Also, the most significant 4 bits (PA4-PA7), are 1's, this corresponds to TTL "High" levels on these lines.

Each digital I/O line on this card has a 10K ohm pull-up resistor to +5 VDC. Therefore, if the above code were executed without any I/O connections, the variable DAT would be 255, or in binary 11111111. The pull-up resistors cause a TTL "High" to be asserted if the line is not forced "Low".

The above examples deal only with PORT A, the first 8 I/O lines. PORTS B, and C on the first 8255 PPI may be read in like manner by substituting BASE + 1, and BASE + 2 respectively, for BASE + 0 in the code. The second 8255 PPI is accessed using BASE + 4, 5 and 6.

To read the status of a *single* bit, the data must be "masked" in software. This is done using the "and" function. Suppose we are interested in knowing if only PA3 is "High" or "Low". The following code will mask the unwanted lines and tell us the state of PA3.

In "GWBASIC"

```
  10 BASE = &H280           ' the dip switch setting on the card
  20 DAT  = INP(BASE + 0)   '                     read PORT A Data
  30 DAT  = DAT  AND 8      ' 8 in binary = 00001000 "PA3 is 8"
  40 IF DAT  = 0 PRINT "PA3 is LOW" ELSE PRINT "PA3 is HIGH"
```

8255 PPI Data Access (Outputs)

The code example in the Initialization section of this manual configures PORT B on the first 8255 PPI as "Outputs". This enables the user to assert a TTL "High" or a TTL "Low" on the I/O lines via software commands. The 8255 is designed so that any PORTS configured as "Outputs" go "Low" after initialization. Changing the state of the I/O lines is much like reading their status, only in the reverse direction. The lines are still accessed in 8 line PORTS and the 8 bits correspond to the 8 I/O lines in the same manner as Inputs.

For an example, we will program PB0 and PB1 to go "High" and PB2 - PB7 to remain "Low".

In "GWBASIC"

```
10 BASE = &H280               ' the dip switch setting on the card
20 DAT = 3
30 OUT BASE + 1, DAT          ' write PORT B Data 3 = 00000011 bin
```

In "Turbo Pascal"

```
const BASE = $280;             {the dip switch setting on the card}
var   DAT  : byte;
 begin
  DAT := 3;
  PORT[BASE + $01] := DAT;     {write PORT B Data 3 = 00000011 bin}
 end;
```

Suppose now that we also want to cause PB6 to go high without disturbing the other 7 lines. This may be accomplished using the "OR" function.

In "GWBASIC"

```
10 BASE = &H280               ' the dip switch setting on the card
20 DAT = DAT OR 64            ' 64 in binary = 0100000 "64 = PB6"
30 OUT BASE + 1, DAT          ' write PORT B Data = 01000011 bin
```

Note that the variable DAT must be maintained to store what was previously written to the PORT. This is because Outputs are "Write only" and may not be read to determine their status. After this code is executed, PB6, PB1 and PB0 will be "High". The remaining lines will still be "Low".

Now lets cause PB1 to go "Low" without disturbing the remaining lines. This is done using the "AND" function.

In "GWBASIC"

```
10 BASE = &H280               ' the dip switch setting on the card
20 DAT = DAT AND 253          ' 253 in binary = 11111101
30 OUT BASE + 1, DAT          ' write PORT B Data
```

Notice that in causing bits to go "Low", the current data is "anded" with all 1's *except* the bit to act upon which is a 0.

8253 CTC Initialization

Just like with the 8255 PPI, the 8253 Counter/Timer Chip (CTC) has several modes of operation, and must be initialized prior to any I/O activity. The most common configuration, Mode 0 - Pulse on Terminal Count, will be discussed here. See the 8253 CTC Data Sheet in Appendix B for more information on other modes of operation.

Note that if +5 VDC power is lost, or the PC is reset, the Control Register must be reinitialized for each counter.

An example of setting the *first* 8253 CTC, Counters 0, 1, and 2 to MODE 0 is as follows:

In "GWBASIC"

```
10 BASE = &H280              ' the dip switch setting on the card
20 OUT BASE + &H0B, &H30     '   counter 0, Mode 0, 2-byte access
30 OUT BASE + &H0B, &H70     '   counter 1, Mode 0, 2-byte access
40 OUT BASE + &H0B, &HB0     '   counter 2, Mode 0, 2-byte access
```

In "Turbo Pascal"

```
const BASE = $280;           {the dip switch setting on the card}
 begin
  PORT[BASE + $0b] := $30; {   counter 0, Mode 0, 2-byte access}
  PORT[BASE + $0b] := $70; {   counter 1, Mode 0, 2-byte access}
  PORT[BASE + $0b] := $b0; {   counter 2, Mode 0, 2-byte access}
 end;
```

An example of setting the *second* 8253 CTC, Counters 0, 1, and 2 to MODE 0 is as follows:

In "GWBASIC"

```
10 BASE = &H280              ' the dip switch setting on the card
20 OUT BASE + &H0F, &H30     '   counter 0, Mode 0, 2-byte access
30 OUT BASE + &H0F, &H70     '   counter 1, Mode 0, 2-byte access
40 OUT BASE + &H0F, &HB0     '   counter 2, Mode 0, 2-byte access
```

In "Turbo Pascal"

```
const BASE = $280;           {the dip switch setting on the card}
 begin
  PORT[BASE + $0f] := $30; {   counter 0, Mode 0, 2-byte access}
  PORT[BASE + $0f] := $70; {   counter 1, Mode 0, 2-byte access}
  PORT[BASE + $0f] := $b0; {   counter 2, Mode 0, 2-byte access}
 end;
```

8253 CTC Access

Once a counter mode has been set, the counter may be loaded, and then read at any time. In the following BASIC program, each counter is loaded using two byte loads, and then read into a variable using two byte reads. Note that the counter data must be latched prior to actually reading the data. This is two insure that there is no counter rollover between the read statements.

8253 CTC Access (continued)

In "GWBASIC"

```
 10 BASE = &H280                   ' the dip switch setting on the card

                                   ' load counter 0 with 65535 (%HFFFF)
 20 OUT BASE + 8, &Hff             ' load counter 0 data (low byte)
 30 OUT BASE + 8, &Hff             ' load counter 0 data (high byte)
                                   ' load counter 1 with 65535 (%HFFFF)
 40 OUT BASE + 9, &Hff             ' load counter 1 data (low byte)
 50 OUT BASE + 9, &Hff             ' load counter 1 data (high byte)
                                   ' load counter 2 with 65535 (%HFFFF)
 60 OUT BASE + &H0A, &Hff          ' load counter 2 data (low byte)
 70 OUT BASE + &H0A, &Hff          ' load counter 2 data (high byte)


                                   ' read counter 0
120 OUT BASE + &H0b, &H00          ' latch counter 0 data
130 DL% = INP(BASE + 8)            ' Read Low Byte counter 0
140 DH% = INP(BASE + 8)            ' Read High Byte counter 0
150 DTA% = (DH% * 256) + DL%'      into one 16 bit integer
                                   ' DTA has the valid counts
                                   ' down from load (65535)
160 DTA% = 65535 - DTA%            ' DTA has number of counts
                                   ' since load on counter 0
170 PRINT DTA%

                                   ' read counter 1
220 OUT BASE + &H0b, &H40          ' latch counter 1 data
230 DL% = INP(BASE + 9)            ' Read Low Byte counter 1
240 DH% = INP(BASE + 9)            ' Read High Byte counter 1
250 DTA% = (DH% * 256) + DL%'      into one 16 bit integer
                                   ' DTA has the valid counts
                                   ' down from load (65535)
260 DTA% = 65535 - DTA%            ' DTA has number of counts
                                   ' since load on counter 1
270 PRINT DTA%

                                   ' read counter 2
320 OUT BASE + &H0b, &H80          ' latch counter 2 data
330 DL% = INP(BASE + &H0A)         ' Read Low Byte counter 2
340 DH% = INP(BASE + &H0A)         ' Read High Byte counter 2
350 DTA% = (DH% * 256) + DL%'      into one 16 bit integer
                                   ' DTA has the valid counts
                                   ' down from load (65535)
360 DTA% = 65535 - DTA%            ' DTA has number of counts
                                   ' since load on counter 2
370 PRINT DTA%
```

8253 CTC Troubleshooting Notes

Loading a counter value, and then immediately reading it back, may not give accurate data. The 8253 CTC requires *1 Clock Pulse* on the CLK input after a load to actually index the data into it's internal registers!

The counter *must* have two successive reads (or writes) if the mode is set for two reads.

The *GATE* line must be high for counting to be enabled. GATE 0 on 8253 CTC #1 is already pulled high on the card. On the other counters, if the gate is not specifically used, a 10k ohm resistor between the gate line and +5 VDC will enable counting. These signals are available on headers J2 and J3.

The 8253 CTC is only capable of counting frequencies to 2.6 Mhz. If greater speeds are needed, an 8254 CTC (Intel) may be substituted, which will allow clock frequencies to 8 Mhz. The 8254 CTC is upward compatible, and operates in the same manner as, the 8253 CTC.

Dip switches 1, 2, and 3 (when ON), will connect the on-board 1 Mhz oscillator to counters 0, 1 and 2 respectively on 8253 CTC #1. If an external clock signal is used, be sure the corresponding switch is OFF.

If a slower frequency than 1 Mhz is needed, counters may be cascaded by simply wire-wrapping the OUT from a counter set up as a square wave generator to the CLK of another counter. See Appendix B for more information on the 8253 CTC Modes and operation.

APPLICATIONS

TTL I/O Interface (Strobed I/O)

Some TTL inputs require a latch (strobe) line for data integrity. This can be accomplished with the DIO Board through software. In the following example, lines PA0-PA7 will be used for a "strobe" and lines PB0-PB7 and PC0-PC7 are used for data input lines. PB0 is the LSB and PC7 is the MSB of a 16 bit data word.

In "GWBASIC"

```
10 BASE = &H280                 'the dip switch setting on the card
                                'Initialization:
                                '(Only done once)
20 OUT (BASE + 3), &H8B         'Set J0, port A to OUTPUTS
                                'J0, port B to INPUTS
                                'J0, port C to INPUTS
30 OUT BASE, &HFF               'Clear J0, port A to OFF

                                'Reading 16 Bit TTL word:
40 OUT BASE, &H00               'Set Latch J0, port A to ON
50 DL% = INP(BASE + 1)          'Read Low Byte on J0, port B
60 DH% = INP(BASE + 2)          'Read High Byte on J0, port C
70 OUT BASE, &HFF               'Clear J0, port A to OFF

                                'Combine Low Byte and High Byte
80 DTA% = (DH% * 256) + DL%     'into one 16 bit integer
                                'DTA has the valid number
```

This program assumes "TRUE HIGH" TTL data. If "TRUE LOW data is required, simply subtract DL% from 255 and subtract DH% from 255 between lines 60 and 70.

BCD (Binary Coded Decimal) data may also be brought in or sent out through the DIO Board. Software routines to convert BINARY to BCD and vice-versa are on the disk provided. If the above example were used for BCD data, a GOSUB call to the BCD conversion routine would be needed after line 80.

Strobed "Outputs" work in somewhat the same manner. First, OUT the data to PORT B and PORT C, and then execute line 30 and then line 70 do provide a "Data Valid" strobe to the external device. This mode of strobing is common when writing data to LED displays.

Optically Isolated I/O Interfacing

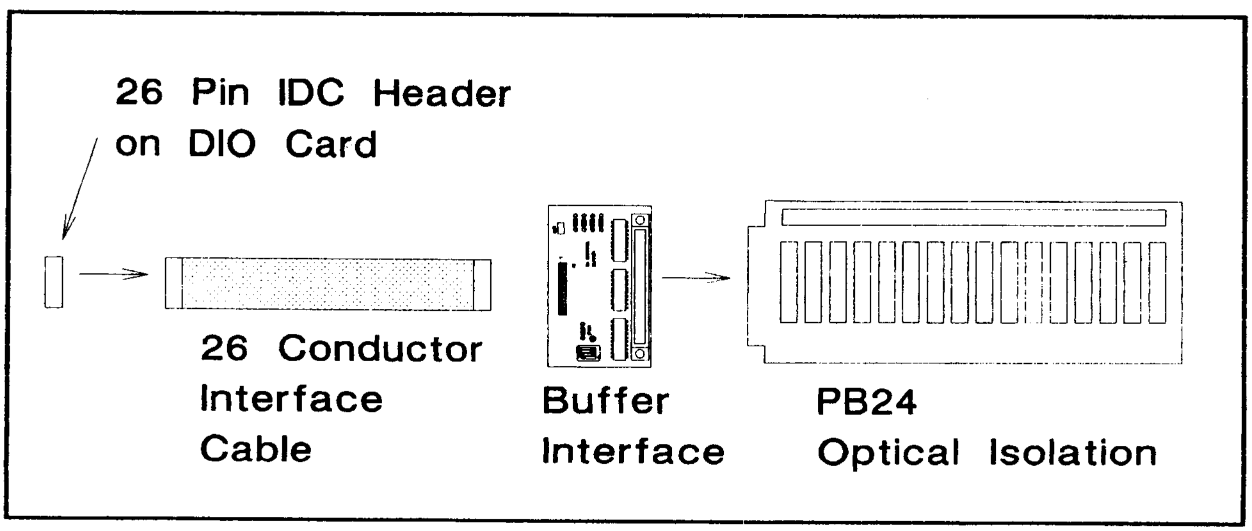
All the Digital I/O cards have the capability for connection to industry standard Input/Output Module Racks. For the most efficient use of I/O space, either a PB24 or PB24Q (OPTO 22, GORDOS etc.) type rack should be used. Each rack has 24 I/O points and corresponds directly to the 24 I/O lines on the 8255 PPI. Typical modules are IAC5, IDC5 (AC and DC inputs), OAC5, ODC5 (AC and DC Outputs). The I/O Modules may be installed as inputs or outputs in groups of eight.

To accomplish interface between the 48 Channel card and the PB24, a *24 line buffer card* (see Options), should be plugged onto the PB24 rack. There are 4 switches on the buffer card. Switch 1, (closest to the edge of the board), must always be on. This enables the rack. The next three switches correspond to the 3 eight module groups on the rack. To configure a group to Inputs, turn the switch OFF. For Outputs, leave the switch ON.

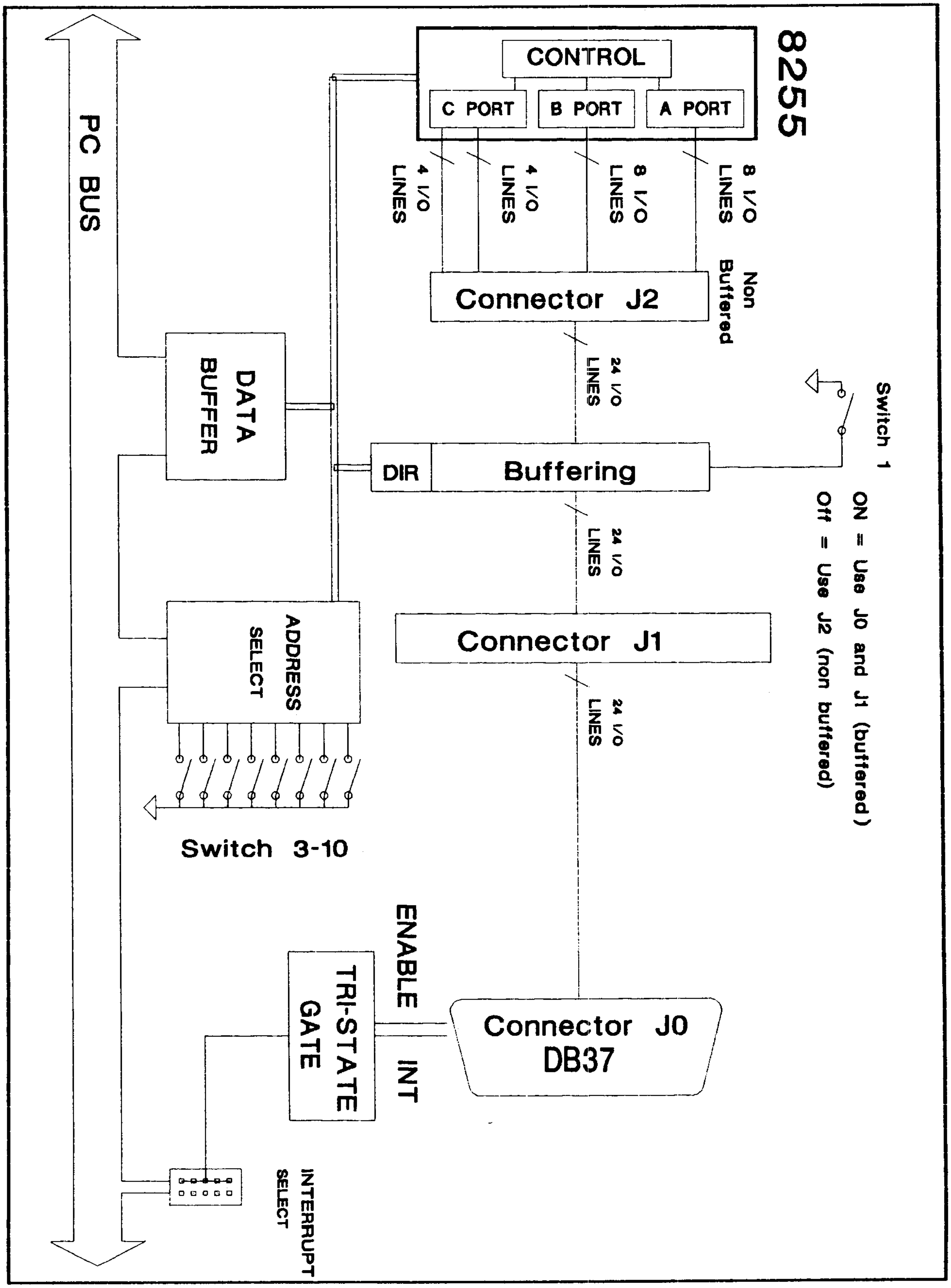
Another version of the PB24 Module Rack (PB24-RK), is available *with buffering* on-board (see Options). Also provided on this version are a Watch Dog Timer, Pluggable Terminal Blocks, and 19" Rack Mounting Capability.

When using either type of Optical Interfacing, note that to turn "ON" an output requires that a "0" bit be programmed into the 8255 PPI. Also when sensing "Inputs", a "0" bit is an indication of the input being in the "ON" state. This convention is considered industry standard practice.

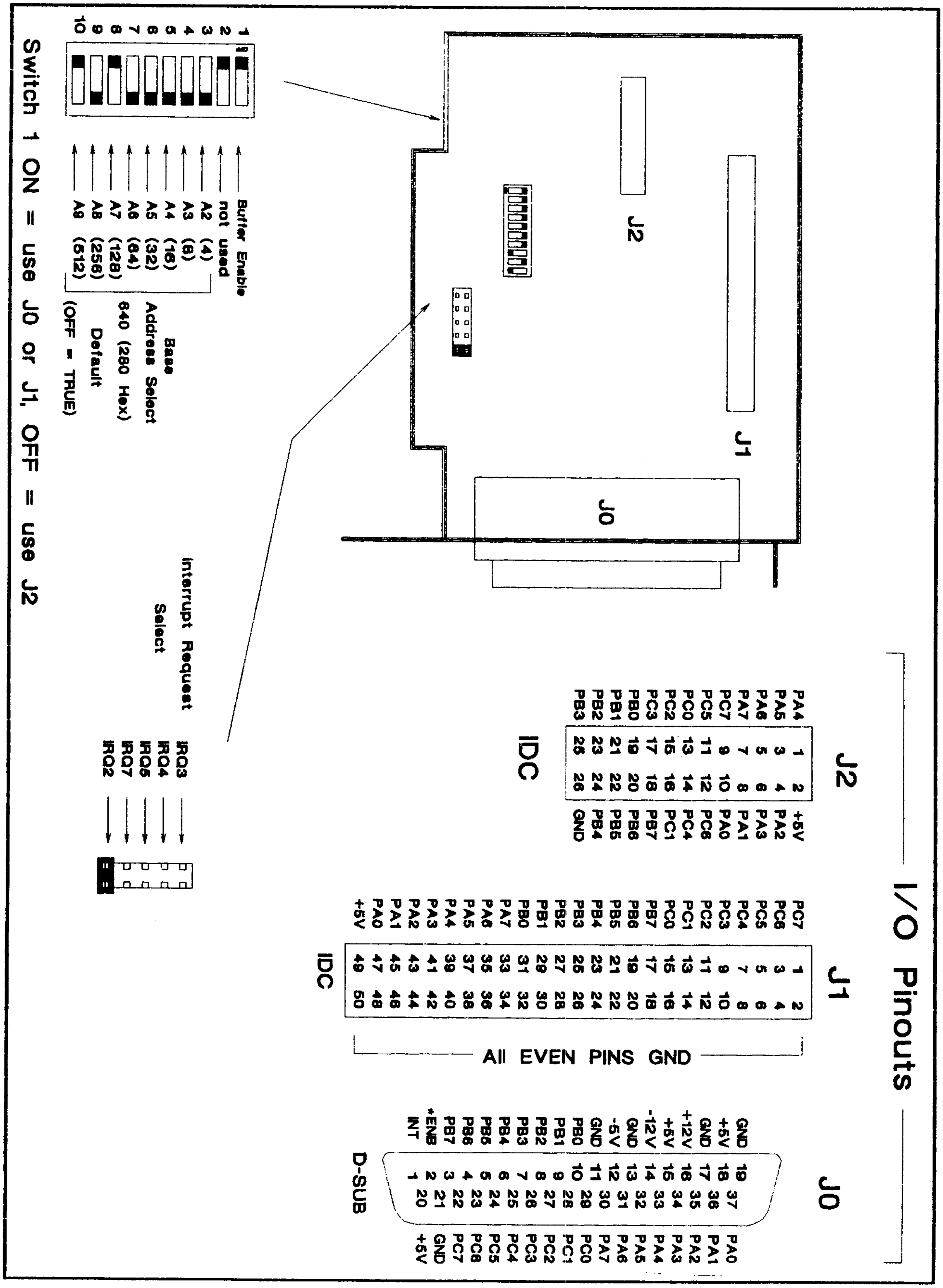
Software routines written in Turbo Pascal, "C" and BASIC, are included with the card. These routines may be incorporated into the application program for access to the I/O modules. Instructions for those routines are included with the source code.



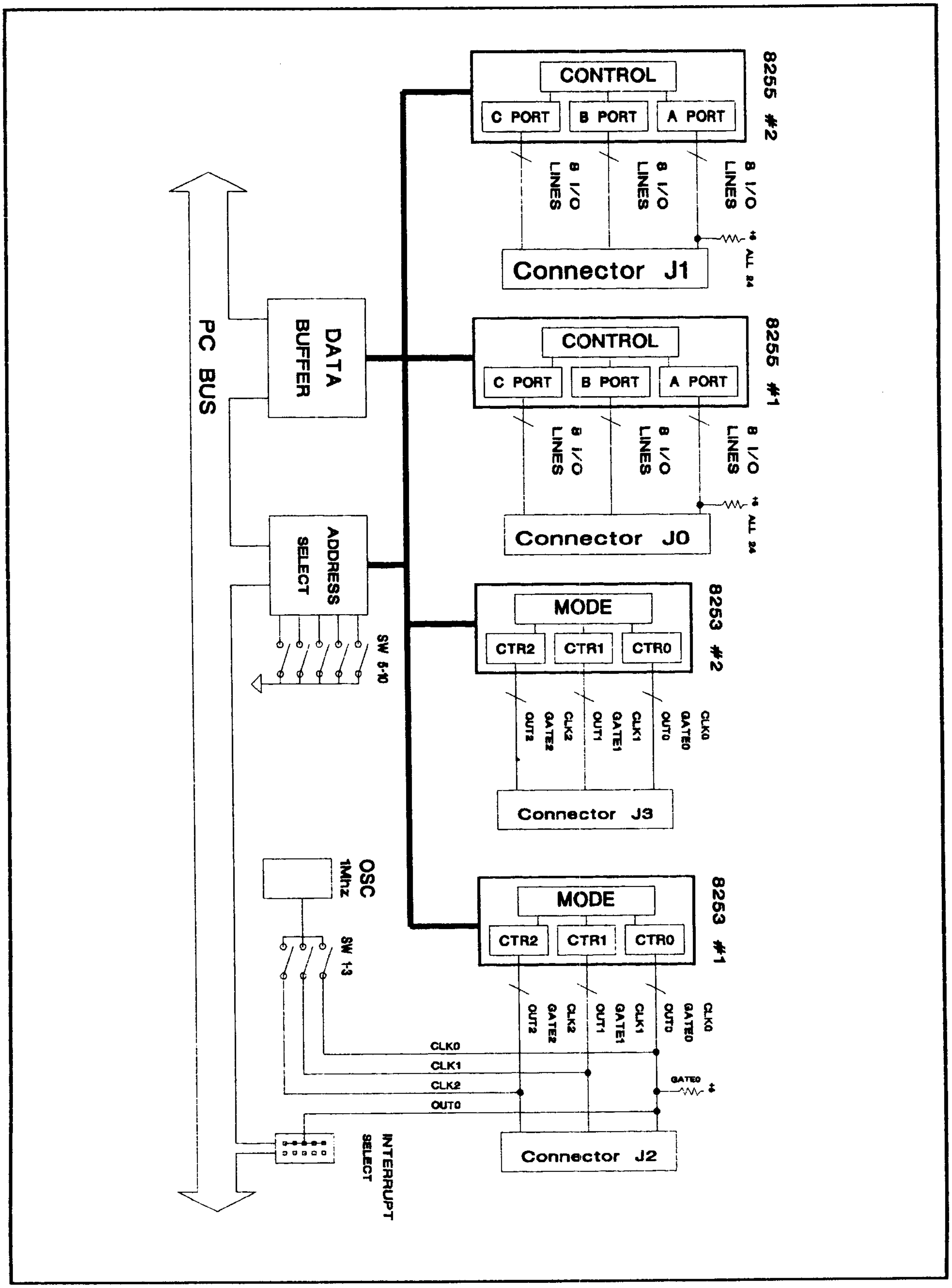
24 Channel – FIGURE 1A – BLOCK DIAGRAM



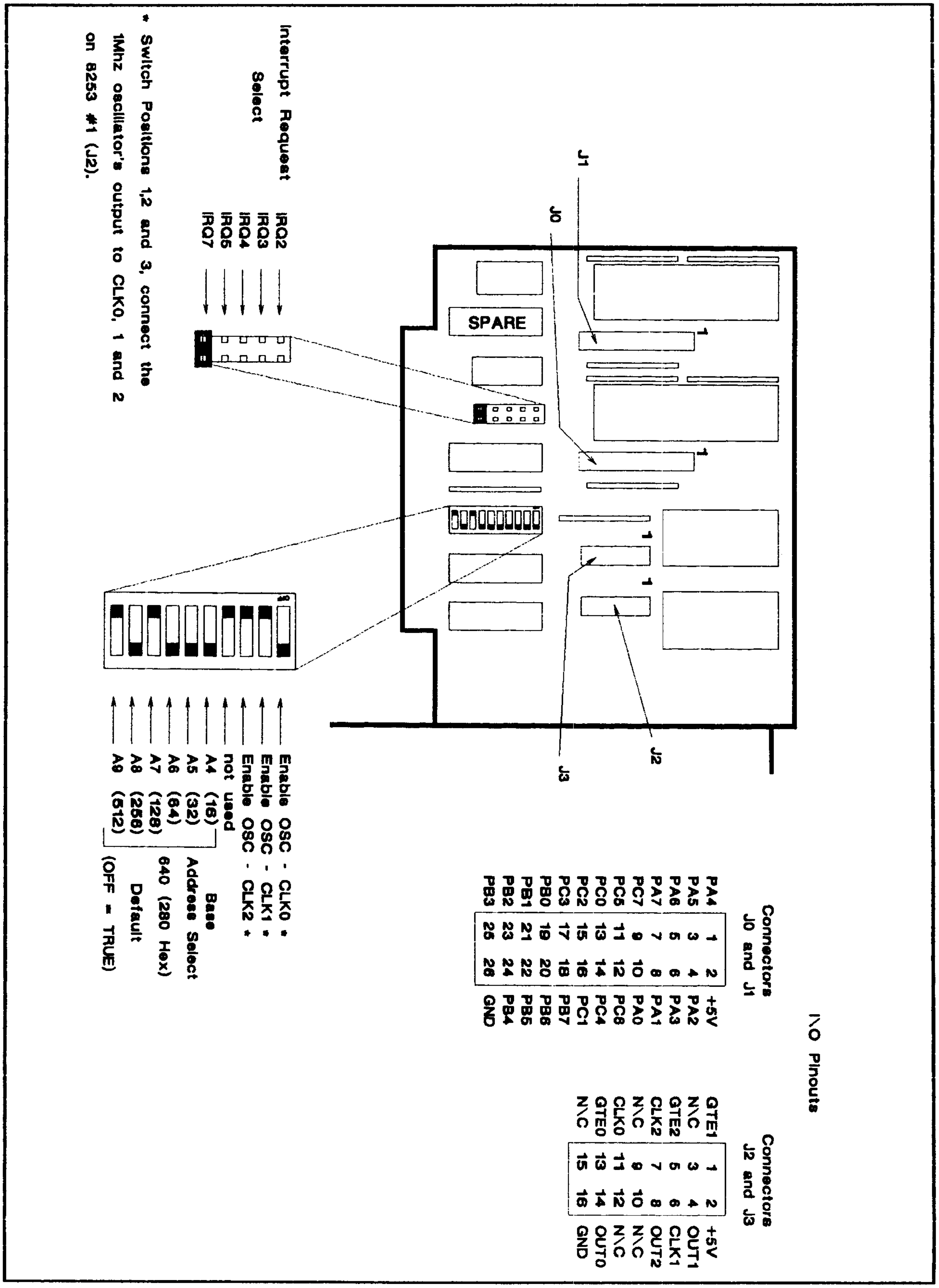
24 Channel – FIGURE 1B – CONFIGURATION



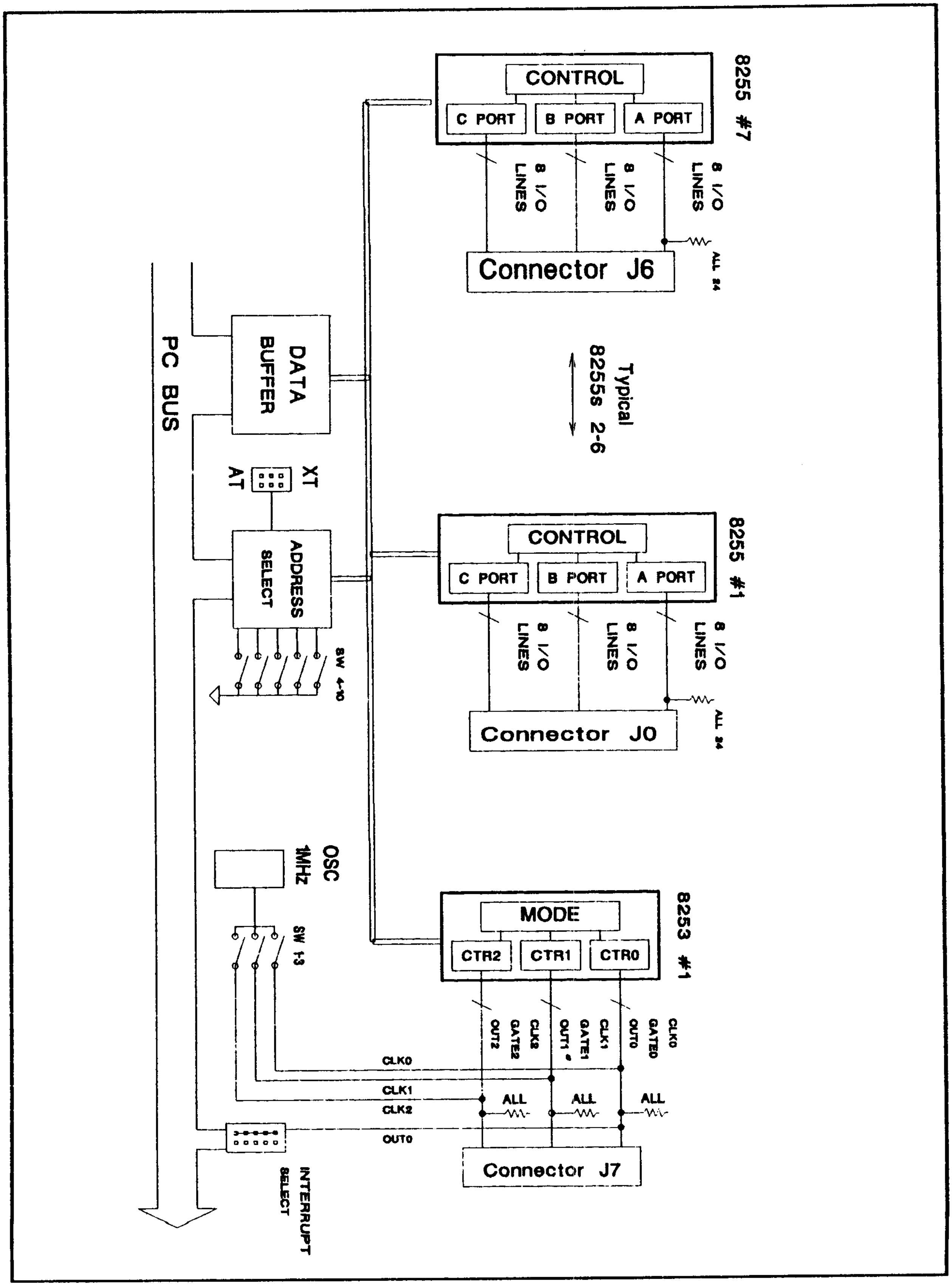
48 Channel – FIGURE 2A – BLOCK DIAGRAM



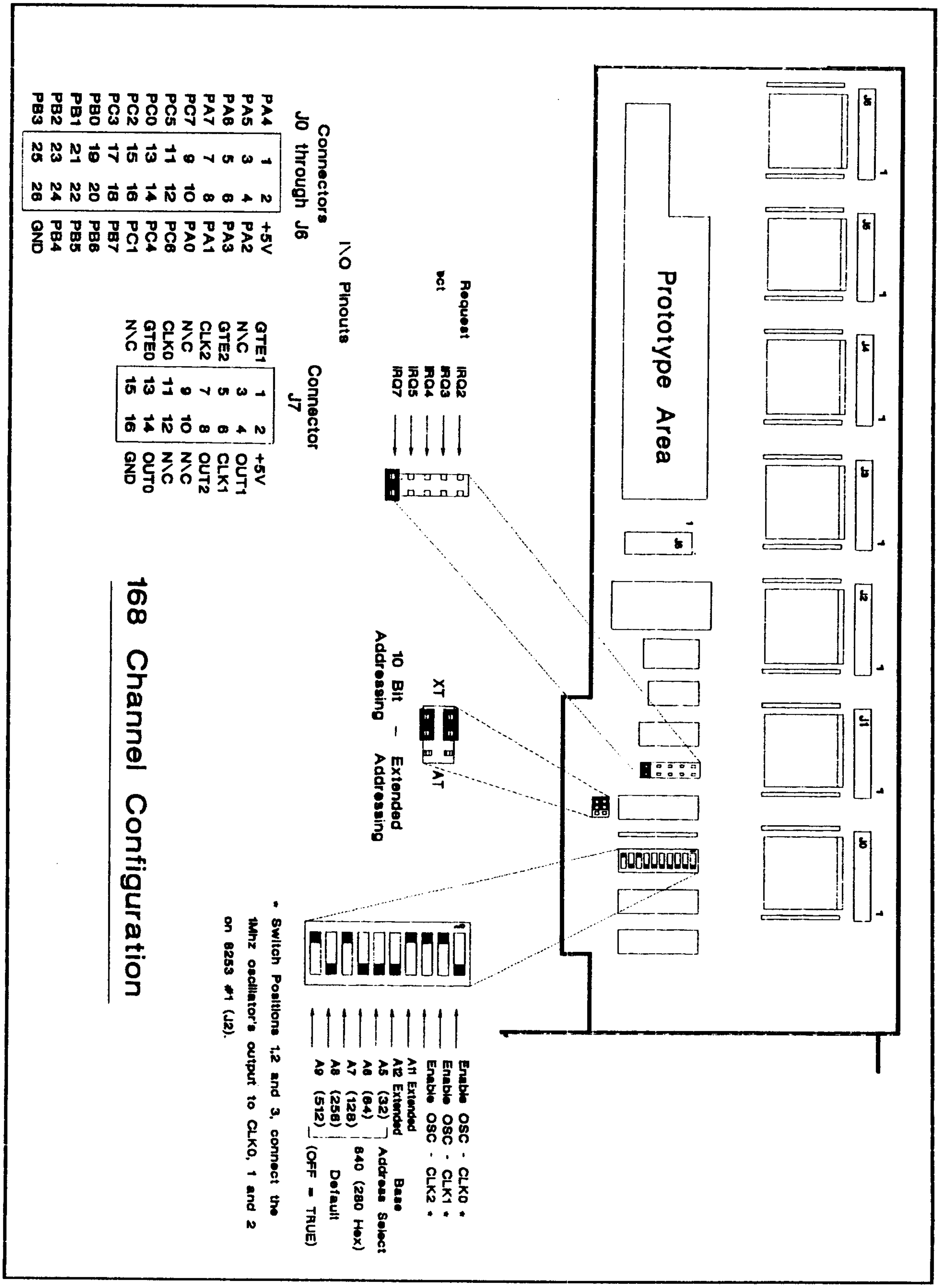
48 Channel – FIGURE 2B – CONFIGURATION



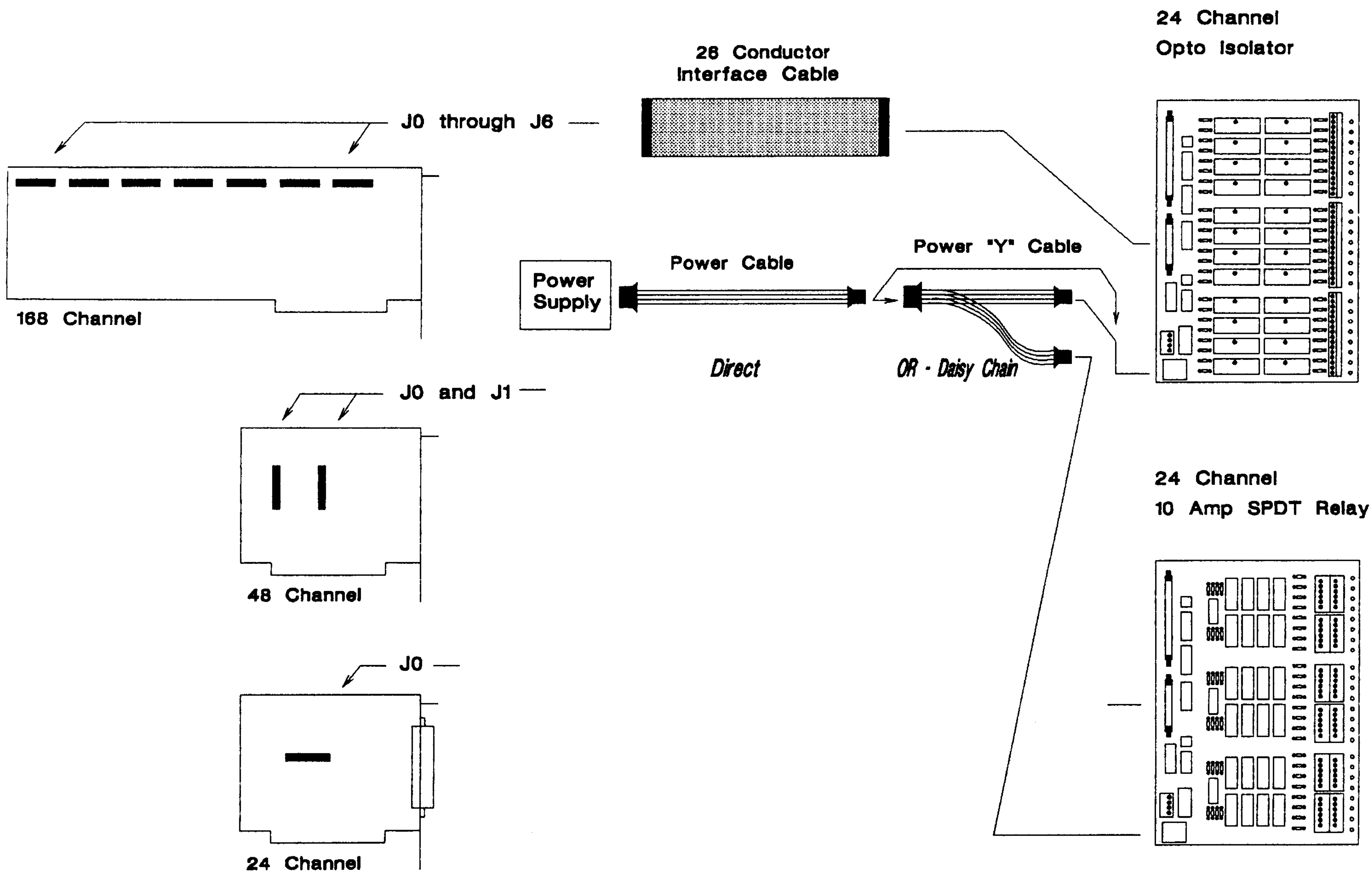
168 Channel - FIGURE 3A - BLOCK DIAGRAM



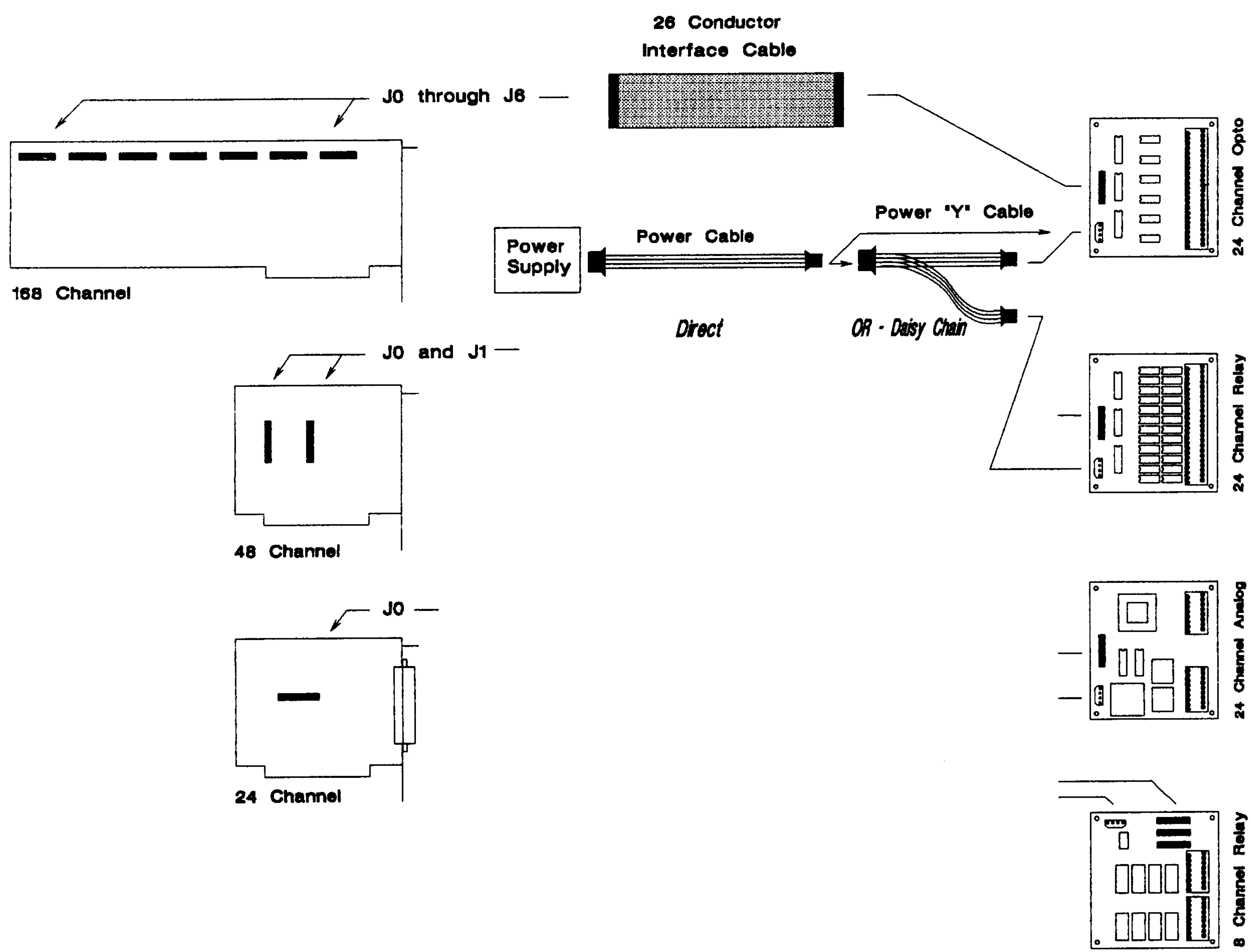
168 Channel - FIGURE 3B - CONFIGURATION



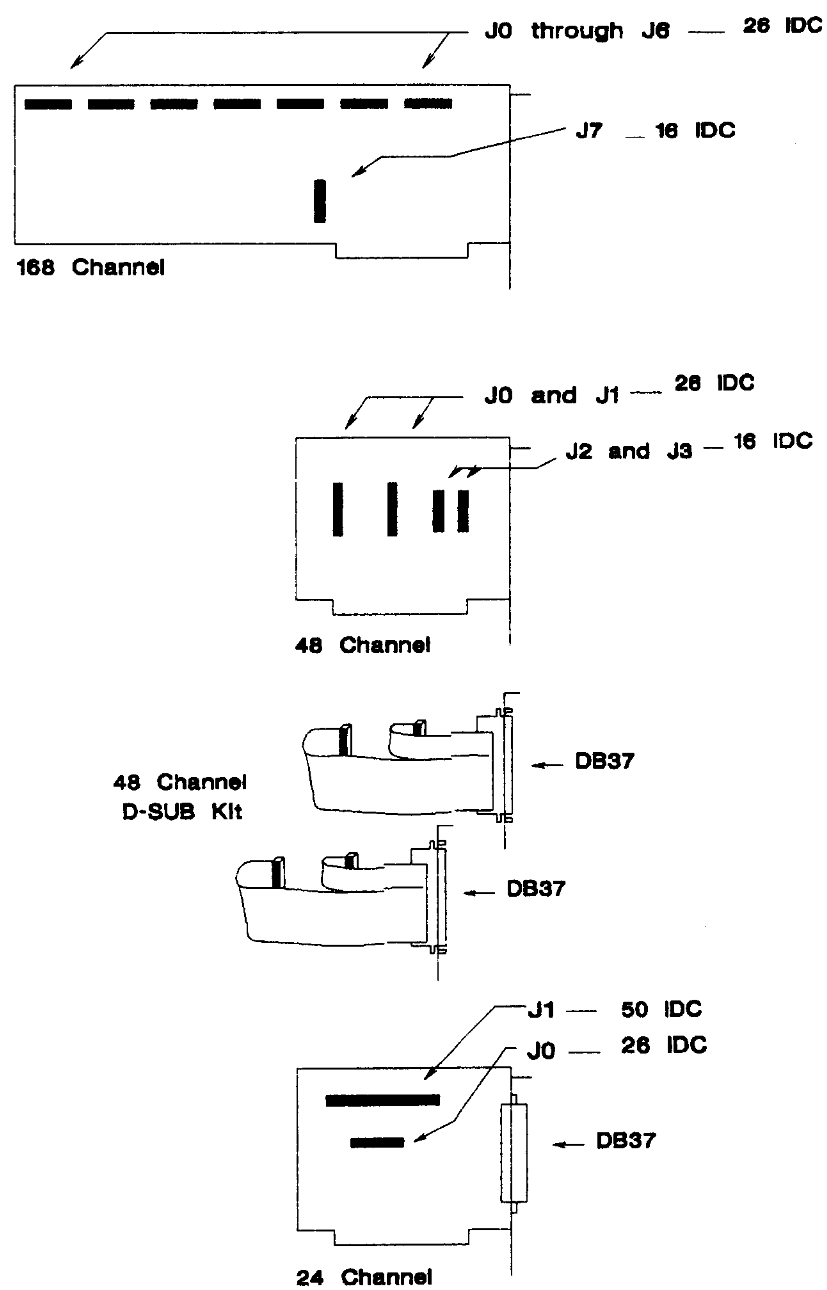
RK Series I/O

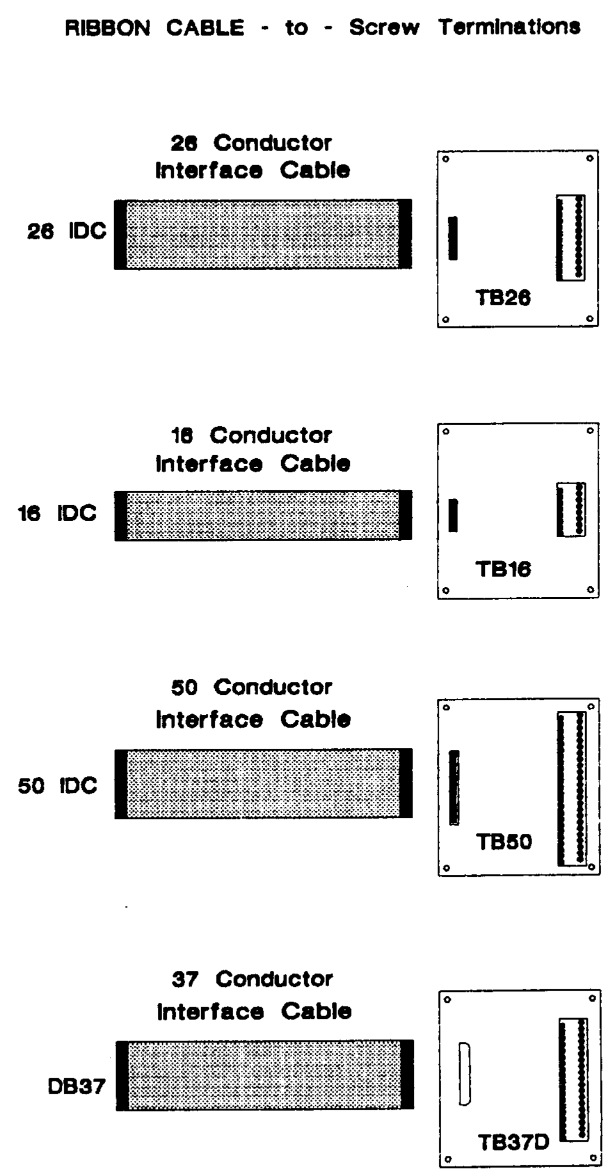


J0 through J6
168 Channel
J0 and J1
48 Channel
J0
24 Channel
26 Conductor Interface Cable
Power Supply
Power Cable
Direct
Power "Y" Cable
OR - Daisy Chain
24 Channel
Opto Isolator
24 Channel
10 Amp SPDT Relay


26 Conductor
Interface Cable
J0 through J6
168 Channel
Power Supply
Power Cable
Power "Y" Cable
Direct
OR - Daisy Chain
J0 and J1
48 Channel
J0
24 Channel
24 Channel Opto
24 Channel Relay
24 Channel Analog
8 Channel Relay

Screw Termination Interfaces





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3. Repair instructions and/or specific problems relative to the product.

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